Curs TFON

Tranzistoare cu Filme Organice si Nanocompozite (TFON)

A. Probleme organizatorice

- Curs – 2h, ziua - orele .... sala ...., titular: Prof. Cristian Ravariu.
- Aplicatii – ....
- Nota finala – 40% tema casa* +20% prez. ** + 40% exam final

- Resurse bibliografice:

  - notite si slide de curs.

  - Articole, Jurnale de specialitate

  Organic Electronics - Elsevier ; Diamond Elsevier; IEEE Transactions on Electron Devices; Journal of Nanomaterials.

- Contact: cristian.ravariu@gmail.com ; sala B108.
- Contact studenti: lista e-mail-uri: .... - pe lista prezenta.

* Pr. / tema de casa – predata cel tarziu in ziua examenului. Format liber (ex. 12 TimesNR, 6-10 pag, cu orice subiect la alegere despre tranzistoare Organice si Nano, DAR NU din slide-urile predate)

** - discutam

A. Prezentare curs

- Curs dedicat sectiei de Master MN.
- Obiective generale :

(1) stabilirea ariei disciplinei TFON in cadrul tranzistoarelor cu filme subtiri actuale,

(2) insusirea tehnologiilor generatoare de materiale nanocompozite si semiconductori organici;

(3) aprofundarea tranzistoarelor cu nano-filme si nanocompozite;

(4) prezentarea tranzistoarelor cu filme organice si a altor dispozitive electronice active cu materiale organice;
(5) abilitati de simulare a dispozitivelor organice

A. Prezentare

- B. Articole publicate de titular in domeniul cursului:

1. **C. Ravariu**. Deeper Insights of the Conduction Mechanisms in a Vacuum SOI Nanotransistor, IEEE Transactions on Electron Devices, vol. 63, no. 8, 2016, pp. 3278 - 3283.

2. **C. Ravariu**, D. Dragomirescu. Different Work Regimes of an Organic Thin Film Transistor OTFT and Possible Applications in Bioelectronics, American Journal of Bioscience and Bioengineering, vol. 3, issue 3-1, June 2015, pp. 7-13.

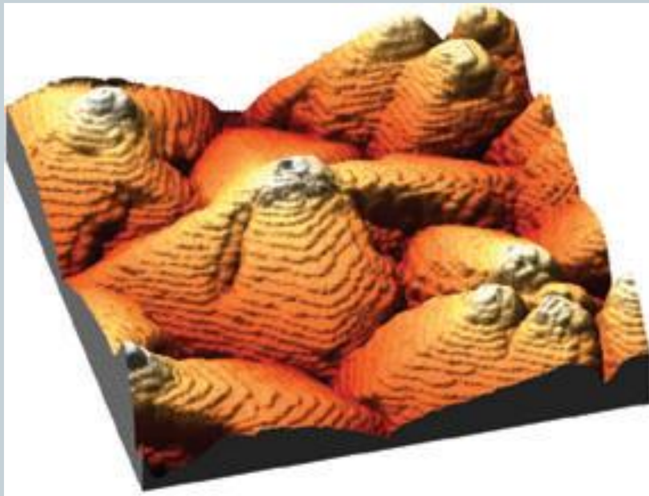
3. **C. Ravariu**, A. Rusu, F. Udrea, et al. Simulation results of some Diamond On Insulator nano-MISFETs, Diamond and Related Materials Elsevier Journal, vol.15, nr.2, pp.777-782, 2006.

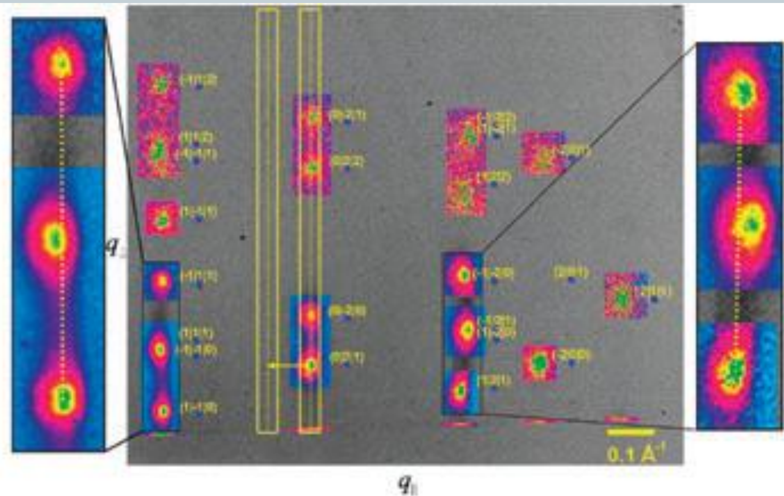
4. **C. Ravariu**. *Compact NOI Nano-Device Simulation*. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, issue 8, Aug 2014, **Page(s):**1841 – 1844.

5. 2017 ....

A. Capitolul 1

Cap. 1. Prezentarea evolutiei tranzistoarelor pe filme organice și nanocompozite





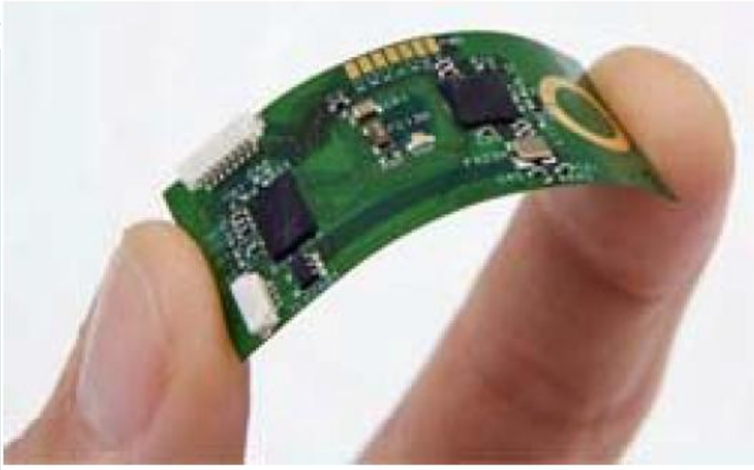
A. Capitolul 1

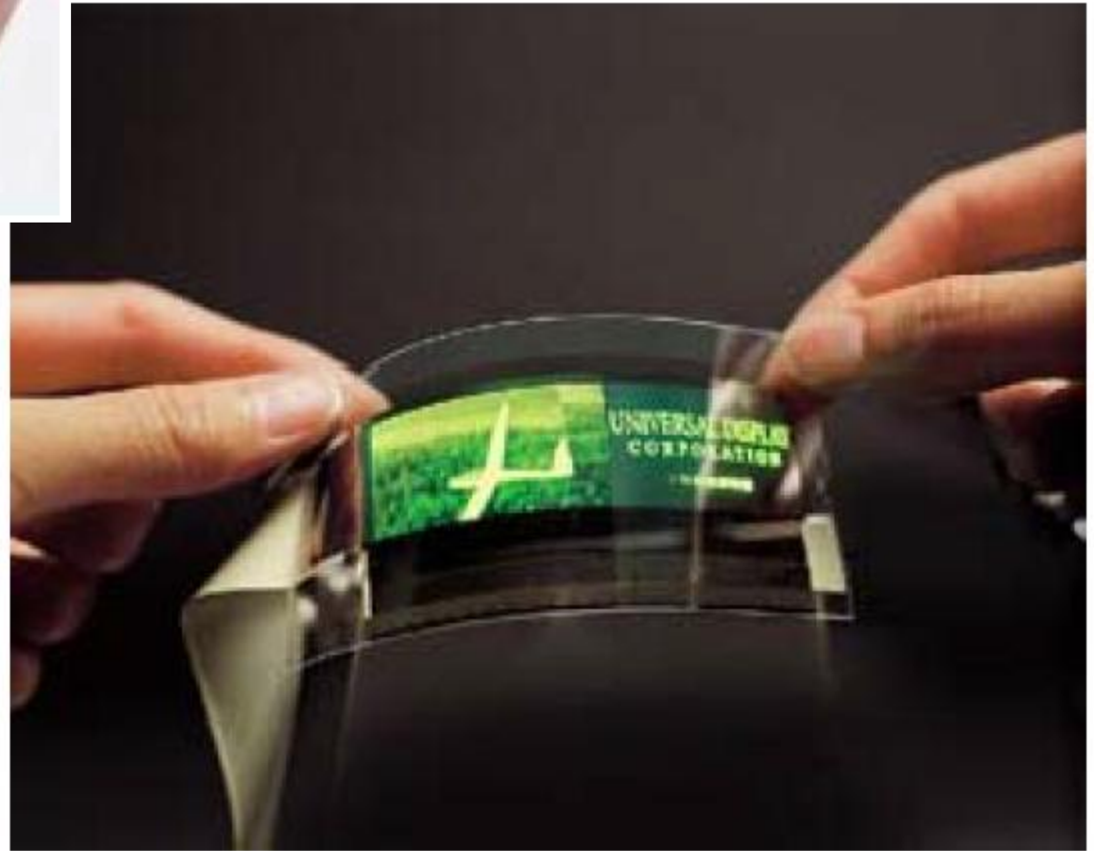
- **Cap. 1. Prezentarea evolutiei tranzistoarelor pe filme organice și nanocompozite**

- 1.1. Repere in electronica organica
- 1.2. Nanocompozite pentru electronica
- 1.3. Incadrarea tranzistoarelor cu filme subtiri TFT

- The TFT concept was patented in 1925 by Julius edger Lilienfeld and in 1934 by Osker Heil but at the time no practical applications has emerged.
- In 1960 several device structures and semiconductor materials like Te, CdSe, Ge and InSb were explored to fabricate TFTs. However, the competition from the MOSFET based on silicon technology forced the TFT to enter in a long period of hibernation.
- In the early 1970s the need for large area applications in flat panel displays motivates the search for alternatives to the crystalline silicon and the TFT found its niche of application.

- In 1979, the hydrated amorphous silicon (a-Si: H) becomes a forerunner as a semiconductor to fabricate TFT.
- Since the mid-1980s, the Si-based TFTs successfully dominated the liquid crystal displays (LCD) technology and become the most important devices for active matrix liquid crystal and organic light emitting diode (OLED) applications.
- In the meantime, TFTs based on organic semiconductor channel layers are introduced in the 1990s.
- Nowadays, organic based thin film transistors (OTFTs) are the candidate for incorporation onto flexible substrates.





- Application 1: fullcolor, video, flexible OLED displays;
- Small OLED displays on conventional glass substrates for mobile phone.
- OTFT technology could be an ideal back-plane for this application due to close materials compatibility OLED – OTFT.

1.1. Repere in electronica organica

- In mainstream semiconductor technology, the MISFET is by far the most important electronic device, forming the backbone of virtually all microprocessors, solid-state memories (DRAM, Flash, etc.), graphics adapters, mobile communication, chips, active-matrix displays, and a wealth of other electronic products.
- In 2010, approximately 10^**19** MISFETs were produced worldwide, with a total value of about 200 billion US-dollars. More than 99% of all MISFETs are manufactured on the surface of single-crystalline silicon wafers.
- Second to the silicon MOSFET in terms of commercial significance is the hydrogenated amorphous SiC Transistor, [1]. [1]. R. A. Street, Adv. Mater., 2009, 21, pag. 2007.

1.1. Repere in electronica organica

- The use of vacuum-deposited films of conjugated small molecule materials for organic semiconductors was pioneered in the late 1980s by Kazuhiro Kudo and co-workers using merocyanines, [24- K. Kudo, M. Yamashina and T. Moriizumi, Jpn. J. Appl. Phys.,1984, vol.23, pp.130], by M. Madru and C. Clarisse using metal phthalocyanines,[26- C. Clarisse, et al, Electron. Lett., 1988, vol. 24, pp. 674] and by Horowitz using oligothiophenes, [27 - G. Horowitz, et al, Solid State Commun., 1989, 72, 381].

1.1. Repere in electronica organica

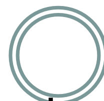
- Organic TFT transistors were first reported in the 1983:
- [A. Tsumura, H. Koezuka and T. Ando, Appl. Phys. Lett., 1986,49, 1210]
- [K. Kudo, M. Yamashina and T. Moriizumi, Jpn. J. Appl. Phys., 1984, 23, 130]
- [F. Ebisawa, T. Kurokawa and S. Nara, J. Appl. Phys., 1983, 54, 3255.]

1.1. Repere in electronica organica

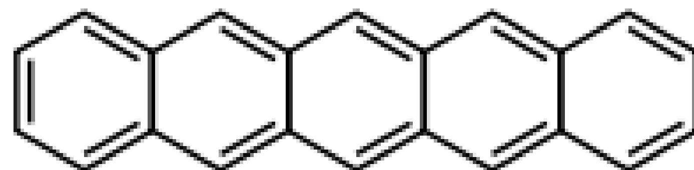
- Initial carrier mobilities were around 0.001cm2/Vs but quickly improved to about 0.1 cm2/Vs, [29- Y. Y. Lin et al, IEEE Trans. Electron Devices, 1997, vol. 44, p.1325].
- In 1997 Tom Jackson predicted and demonstrated that the carrier mobility of many organic semiconductors can be substantially improved by growing the films on low-energy surfaces, [30 -Y. Y. Lin, D. J. Gundlach, S. F. Nelson and T. N. Jackson, IEEE Electron Device Lett., 1997, 18, 606].

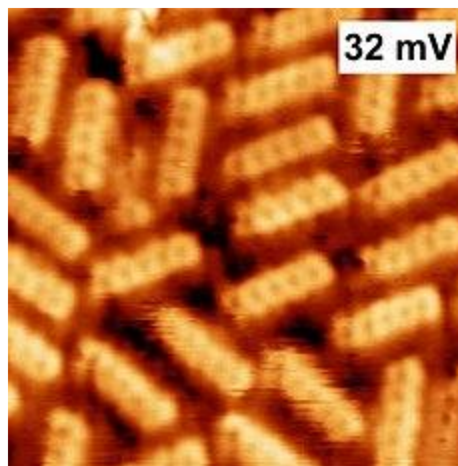
1.1. Repere in electronica organica

- The concept of improving the carrier mobility in organic semiconductor films by controlling the semiconductor film growth using self-assembled monolayers, which was initially demonstrated for small-molecule semiconductors [29,30] was later also extended to polymeric semiconductors, [39 - A. Salleo et al, Appl. Phys. Lett., 2002, vol81, pp4383.].
- Although a substantial number of small-molecule semiconductors have emerged, pentacene consistently provides the largest carrier mobilities.



Pentacene is a polycyclic aromatic hydrocarbon with five linearly-fused benzene rings



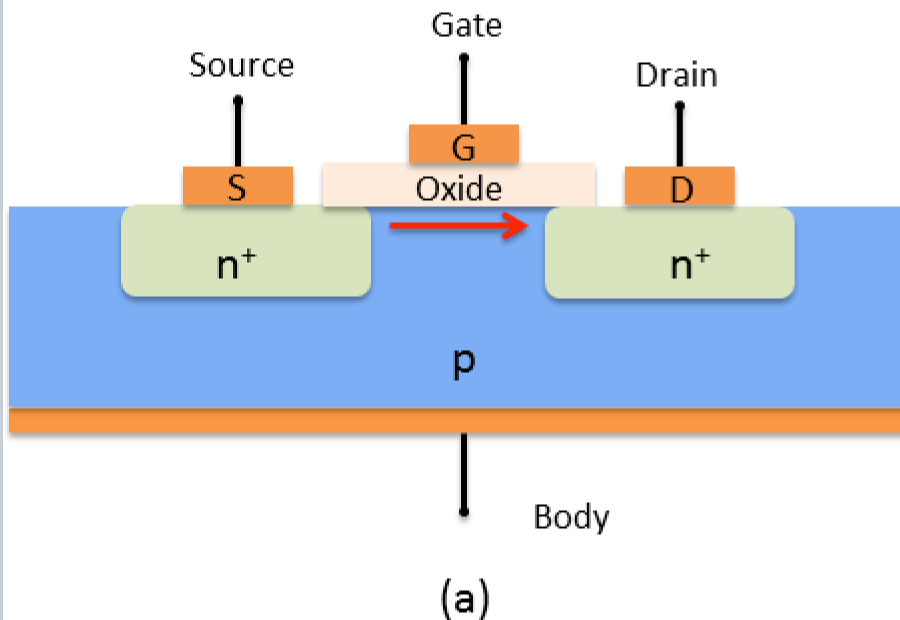


Scanning tunneling microscopy image of pentacene molecules on nickel, [*].

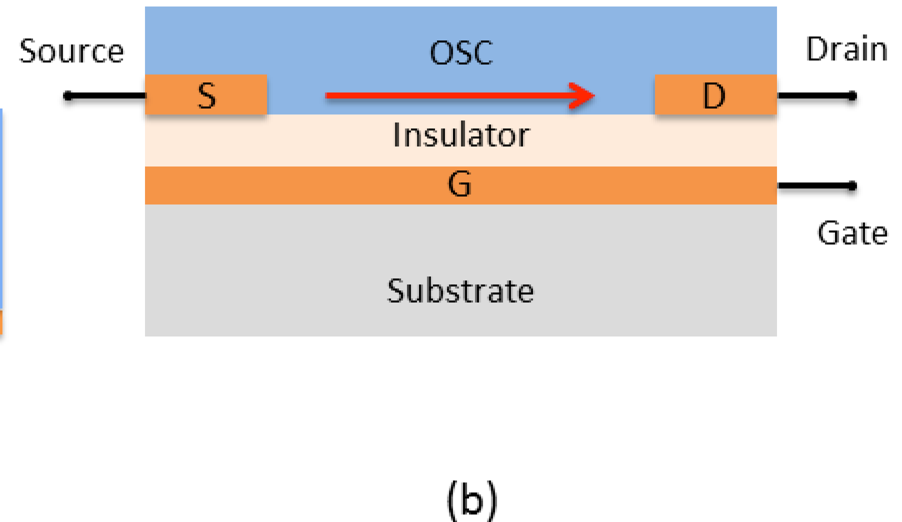
[*]. Dinca, et al (2015). "Pentacene on Ni(111): Room-temperature molecular packing and temperature-activated conversion to graphene". *Nanoscale*. **7** (7): pp. 3263–3269.

- A TFT is formed by placing thin films of the dielectric layer as well as an active semiconductor layer and metallic contacts onto a supporting substrate.
- TFT and MOSFET operation is similar in that the current from the source to the drain terminal is modulated by the applied gate electric field.
- Current modulation in a TFT or in a MISFET can be explained if the metal-insulator-semiconductor (MIS) part of the TFT is considered as a capacitor.

- Fig. 1 shows a cross-sectional schematic drawing of a MOSFET and a TFT.



(a)

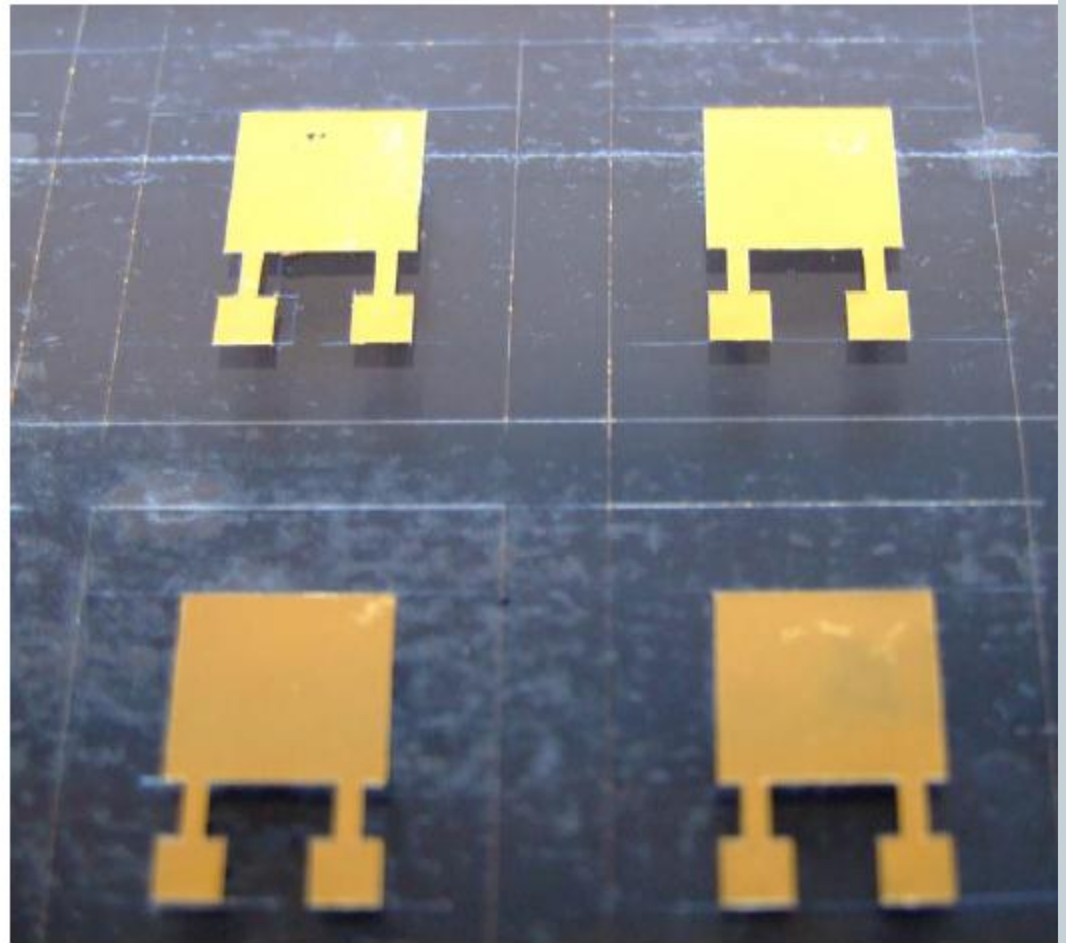


(b)

1.1. Repere in electronica organica

- 2009 – Romania

Electrozi de Au depusi pe suport flexibil.



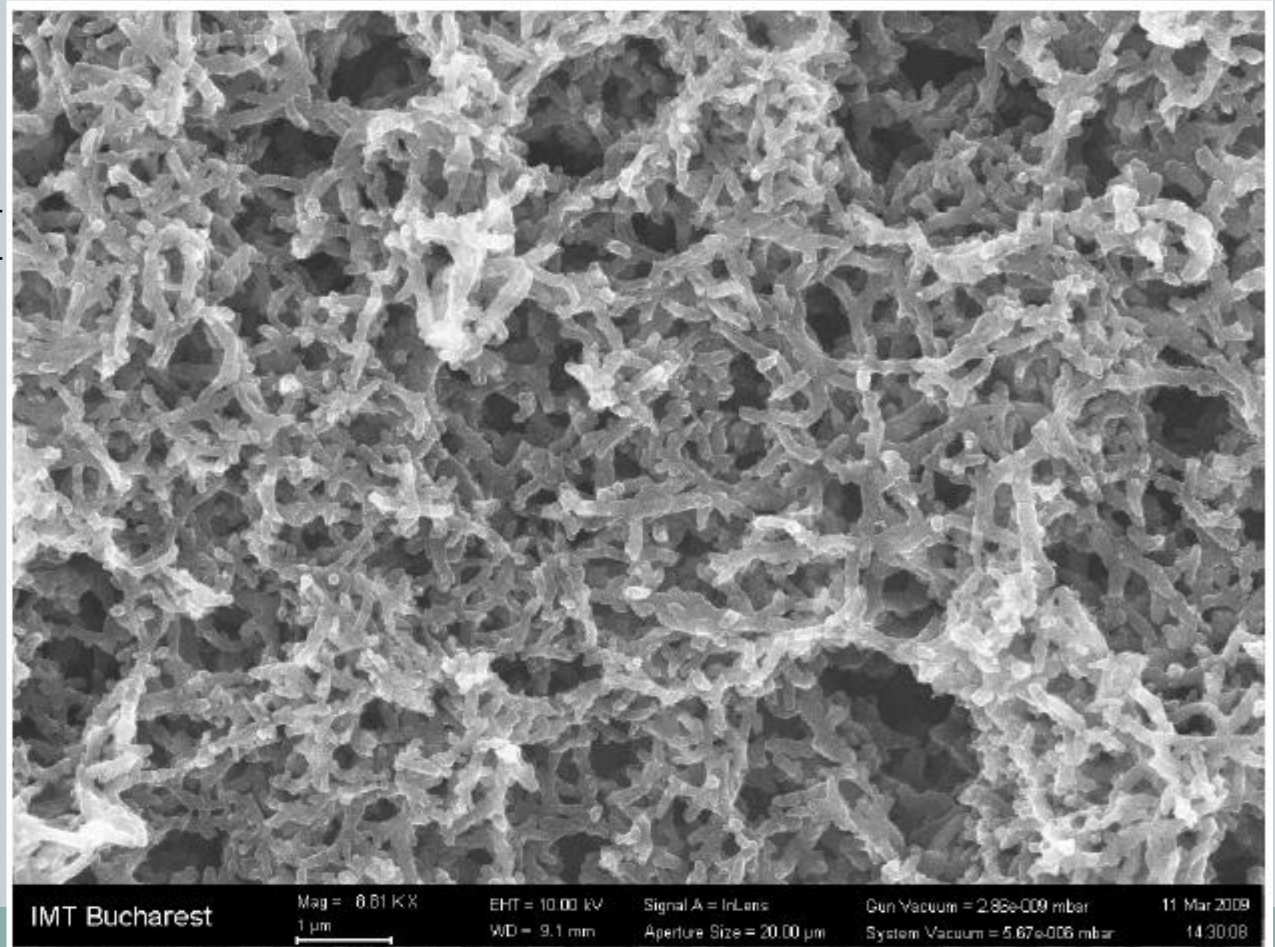
1.1. Repere in electronica organica

- La IMT – au fost realizati electrozi de Au pe polianilina.

Structura SEM

a polianilinei

scala 1um



1.1. Repere in electronica organica

- Anilina scala 200nm

1.1. Repere in electronica organica

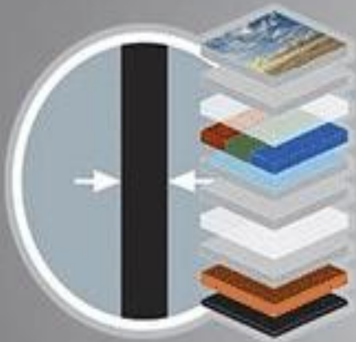
- 2011- 2017

1.1. Repere in electronica organica

1.1. Repere in electronica organica

1.1. Repere in electronica organica

LED



OLED

A TV with conventional LED technology requires a backlight unit (known as a BLU) to generate light that passes through the coloured pixels.

An OLED TV possesses organic sub-pixels that generate their own light. Because of this, they do not require a backlight unit - making OLED TVs thinner than conventional LED TVs.

1.2. Nanocompozite pentru electronica

- Domeniu in formare – permite mai multe directii:

- scala nano-metrica pentru dispozitive;

- compusi chimici care au nano-granulatii si se aplica in DE;

- De fapt "nanocompozite" – materiale care detin domenii la scala nanometrica ce se repeta pe cele 3 axe. Nano-domeniile au sub-100nm.

Exemple: materiale nano-poroase, geluri, coloizi, co-polimeri, combinatii solide intre o matrice de volum si faze nano-dimensionale.

1.2. Nanocompozite pentru electronica

348 IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 3, MARCH 2012

Mobility Enhancement by Back-Gate Biasing in Ultrathin SOI MOSFETs With Thin BOX

A. Ohata, *Member, IEEE*, Y. Bae, C. Fenouillet-Beranger, and S. Cristoloveanu, *Fellow, IEEE*

***Abstract*—Carrier mobility (μ) at various back-gate biases is studied for n- and p-channel ultrathin (8 nm) SOI MOSFETs with thin (10 nm) buried oxide (BOX) and ground plane (GP). We found that μ did not deteriorate for either thin BOX or GP structure, even in the back channel (BC). We also found the largest μ enhancement effect in p-channel devices by the back-gate bias. As this enhancement effect could conceal the superior μ at the Si/SiO_2 interface, μ was maximized when both the front channel and BC were conducting. By contrast, μ in n-channel devices was maximized only when the BC was activated. This large μ gain in p-channel devices is promising for further CMOS scaling.**

***Index Terms*—Back gate, mobility, MOSFET, silicon-on-insulator (SOI), thin buried oxide (BOX), ultrathin film.**

I. Introduction

TO SCALE the gate length in MOSFETs while controlling short-channel effects, the thicknesses of silicon-on-

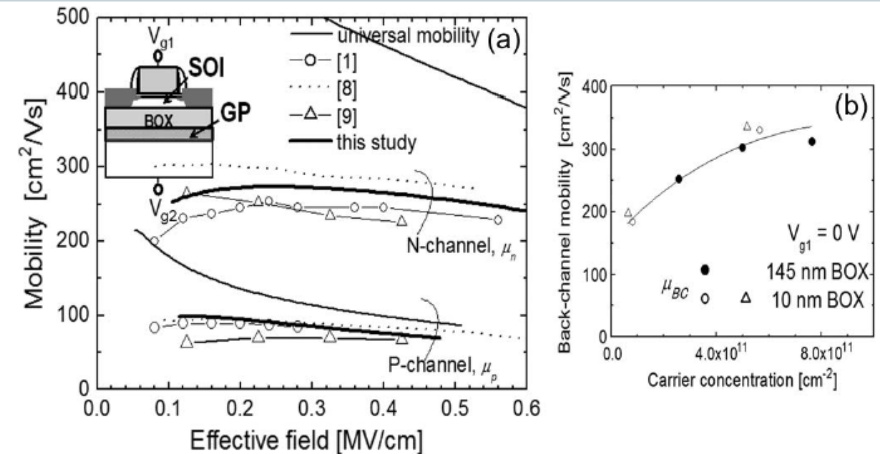


Fig. 1. (a) Bold lines show μ_n and μ_p at $V_{g2} = 0$ V for SOI MOSFETs. Devices with channel length/width of 10/10 μm were used. μ_n and μ_p from several previous reports [1], [8], [9] were also plotted. In [8], T_{SOI} over thick BOX was 14 nm. In [9], $T_{SOI} = 20$ nm, and $T_{BOX} = 145$ nm. In [1], $T_{SOI} = 8-10$ nm, $T_{BOX} = 20$ nm, and GP structure. In [1], [8], and [9], high-k/metal

1.2. Nanocompozite pentru electronica

APPLIED PHYSICS LETTERS **100**, 093112 (2012)

Scaling of Al_2O_3 dielectric for graphene field-effect transistors

B. Fallahazad,[1,a)] K. Lee,[1] G. Lian,[2] S. Kim,[1] C. M. Corbet,[1] D. A. Ferrer,[1] L. Colombo,[2] and E. Tutuc[1]
[1]*Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA*
[2]*Texas Instruments Incorporated, 13121 TI Boulevard, Dallas, Texas 75243, USA*

(Received 7 October 2011; accepted 3 February 2012; published online 1 March 2012)

We investigate the scaling of Al_2O_3 dielectric on graphene by atomic layer deposition (ALD) using ultra-thin, oxidized Ti and Al films as nucleation layers. We show that the nucleation layer significantly impacts the dielectric constant (k) and morphology of the ALD Al_2O_3, yielding $k = 5.5$ and $k = 12.7$ for Al and Ti nucleation layers, respectively. Transmission electron microscopy shows that Al_2O_3 grown using the Ti interface is partially crystalline, while Al_2O_3 grown on Al is amorphous. Using a spatially uniform 0.6 nm-thick Ti nucleation layer, we demonstrate graphene field-effect transistors with top dielectric stacks as thin as 2.6 nm. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3689785]

1.2. Nanocompozite pentru electronica

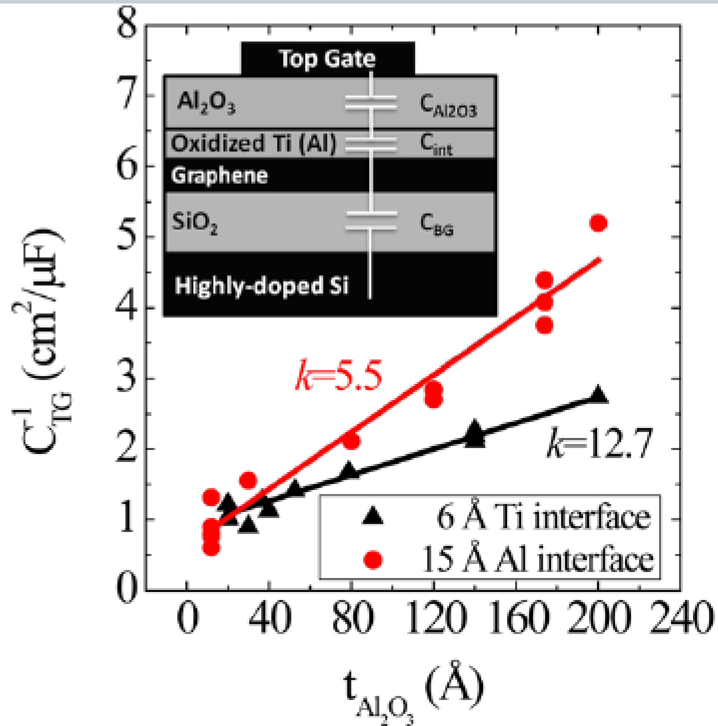
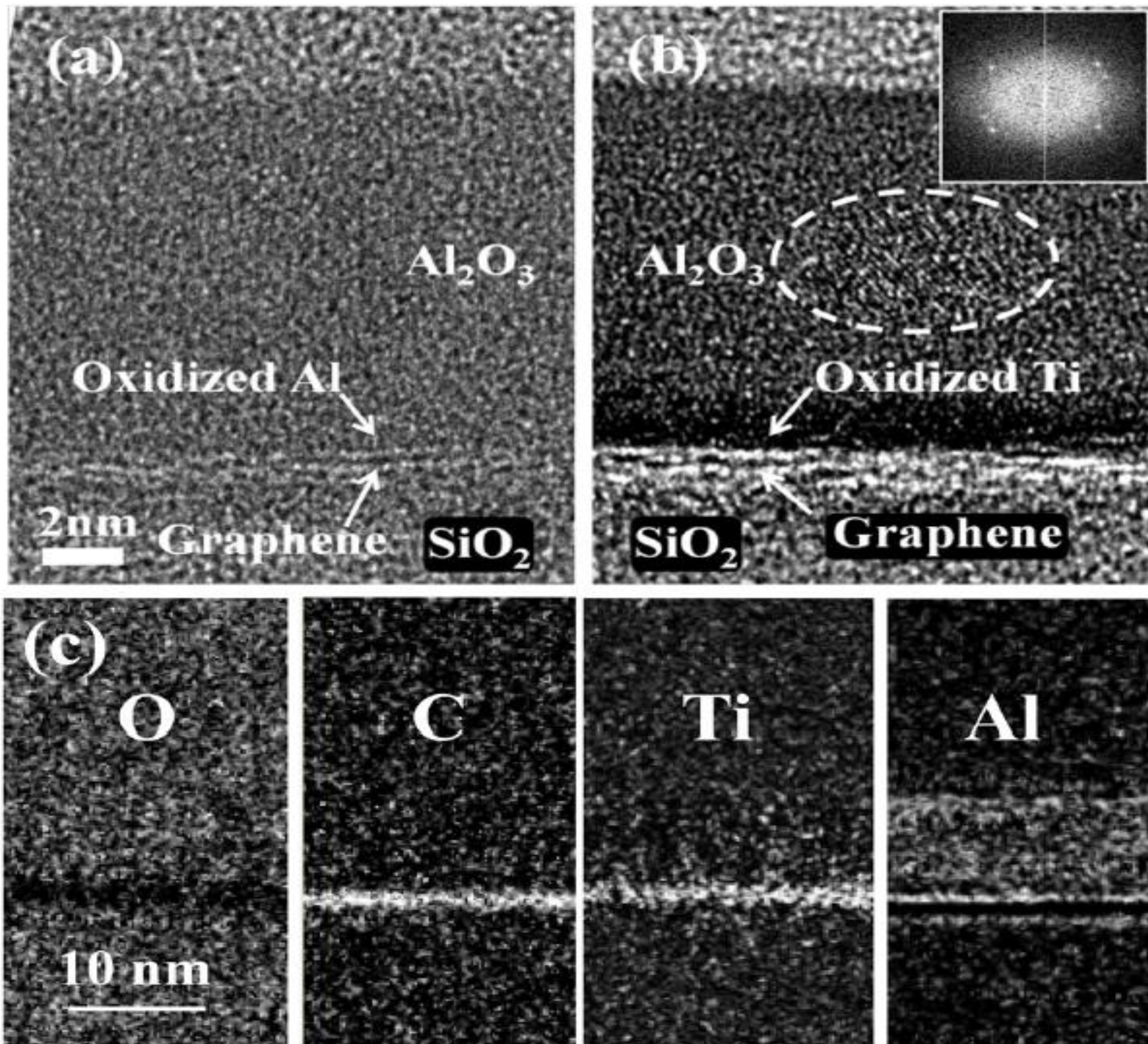


Fig de pe pag urmatoare va arata:

FIG. TEM cross section micrographs of ALD Al_2O_3 on graphene, grown using Al (a) and Ti (b) nucleation layers. Panel (b) inset: Fast Fourier transform corresponding to the grain marked by the dashed line. (c) Compositional maps of oxygen, carbon, titanium, and aluminum determined from EELS measurements on an Al_2O_3/TiO_x/graphene stack.

Appl. Phys. Lett. **100**, 093112 (2012)



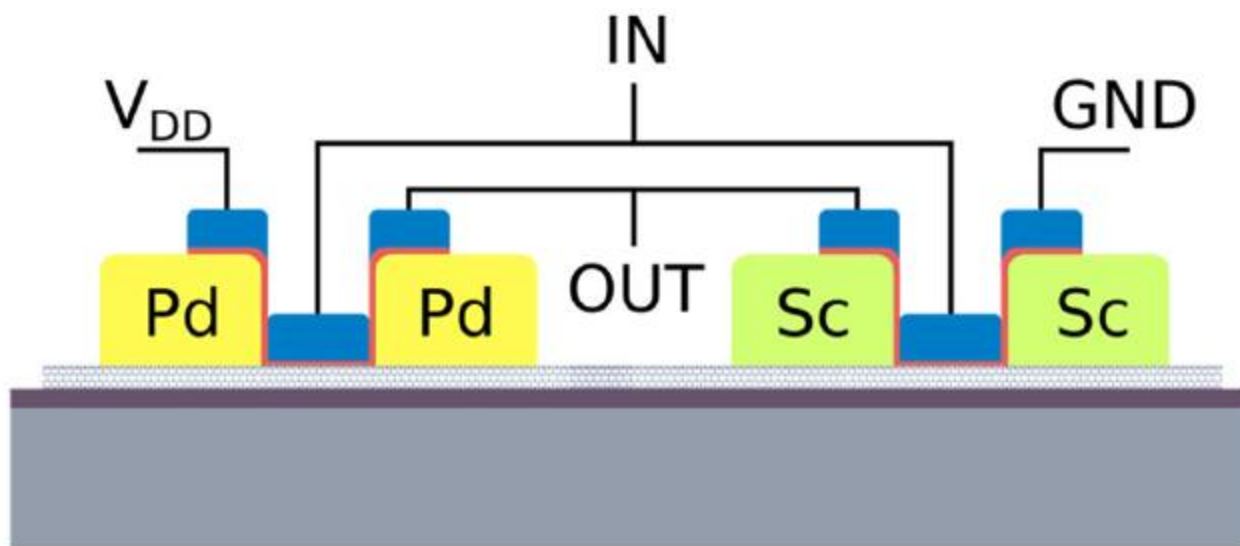
APPLIED PHYSICS LETTERS **100**, 263116 (2012)

Carbon nanotube based ultra-low voltage integrated circuits: Scaling down to 0.4 V

Li Ding,[1] Shibo Liang,[1] Tian Pei,[1] Zhiyong Zhang,[1,a)] Sheng Wang,[1] Weiwei Zhou,[2] Jie Liu,[2] and Lian-Mao Peng[1,a)]
[1]*Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China*
[2]*Department of Chemistry, Duke University Durham, North Carolina 27708, USA*

(Received 14 May 2012; accepted 12 June 2012; published online 29 June 2012)

Carbon nanotube (CNT) based integrated circuits (ICs) including basic logic and arithmetic circuits were demonstrated working under a supply voltage low as 0.4 V, which is much lower than that used in conventional silicon ICs. The low limit of supply voltage of the CNT circuits is determined by the degraded noise margin originated from the process inducing threshold voltage fluctuation. The power dissipation of CNT ICs can be remarkably reduced by scaling down the supply voltage, and it is of crucial importance for the further developments of nanoelectronics ICs with higher integration density. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4731776]



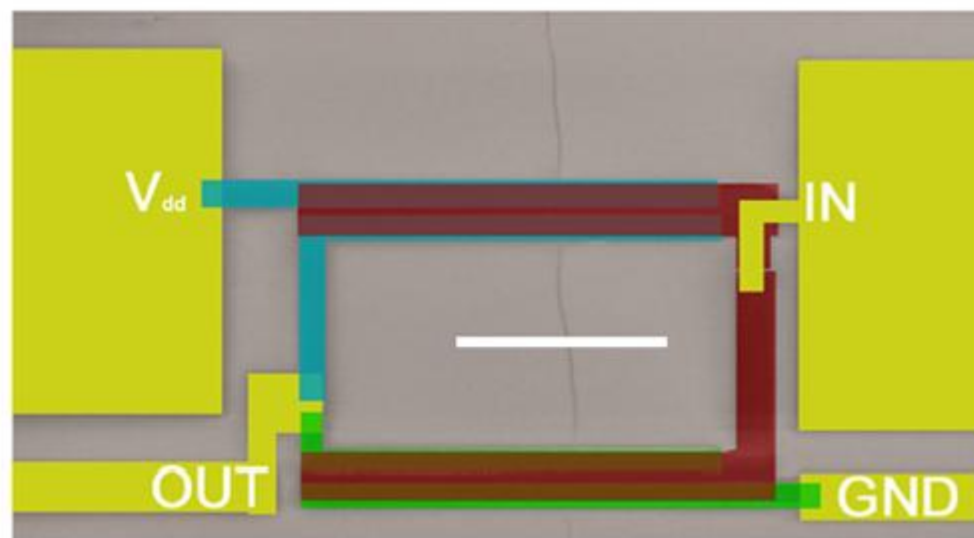


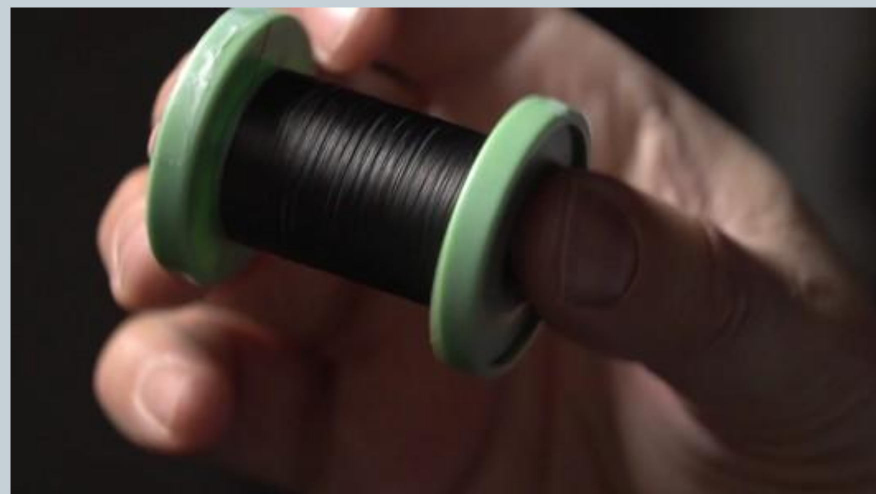
FIG. 1. (a) Schematic and (b) SEM image of a CNT based CMOS inverter with a pair of p- and n-FETs.

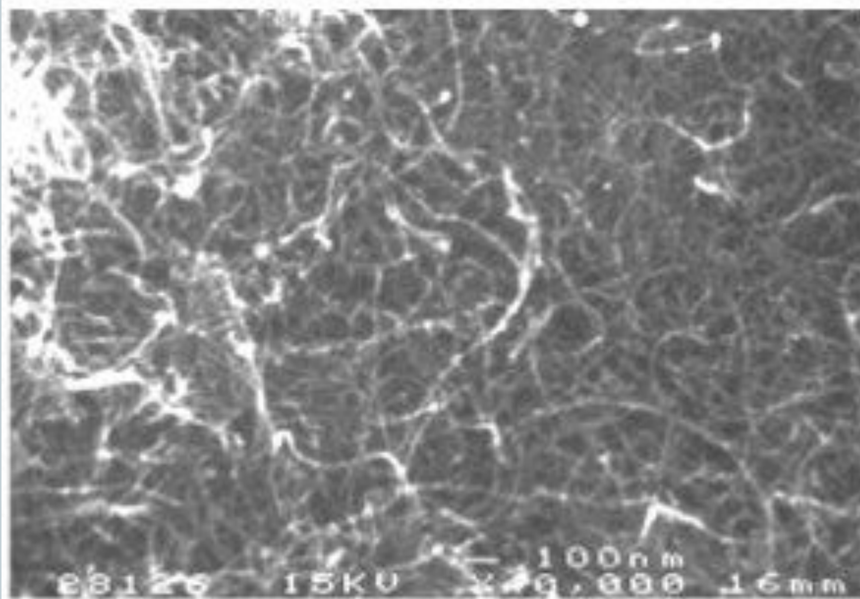
Chapter 29
In Tech

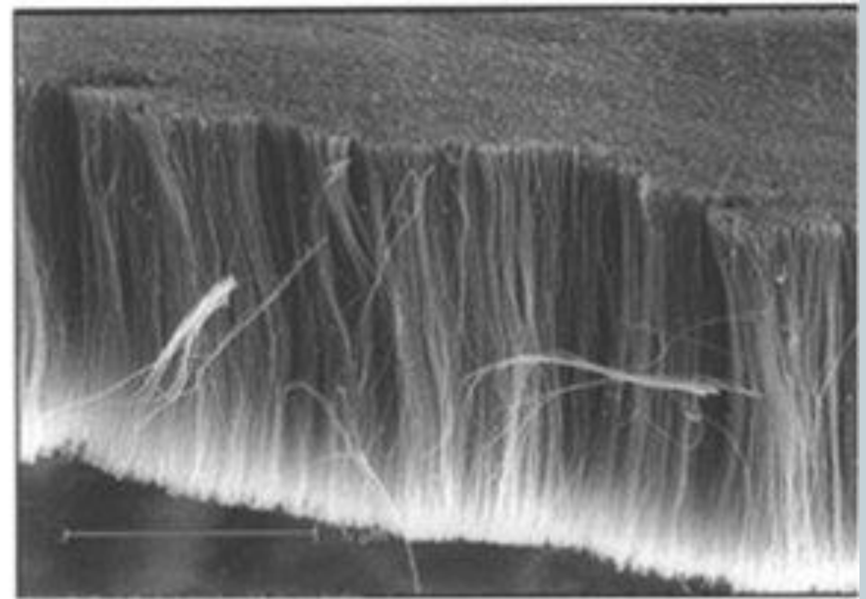
OPEN ACCESS

Carbon Nanotube Supercapacitors

Wen Lu[1] and Liming Dai[2]







Scanning electron microscopic (SEM) images of (a): randomly entangled CNTs (Niu et al., 1997), and (b): vertically aligned CNTs (Huang et al., 1999).

APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

Porous silicon for electrical isolation in radio frequency devices: A review

G. Gautier[1,a)] and P. Leduc[2]
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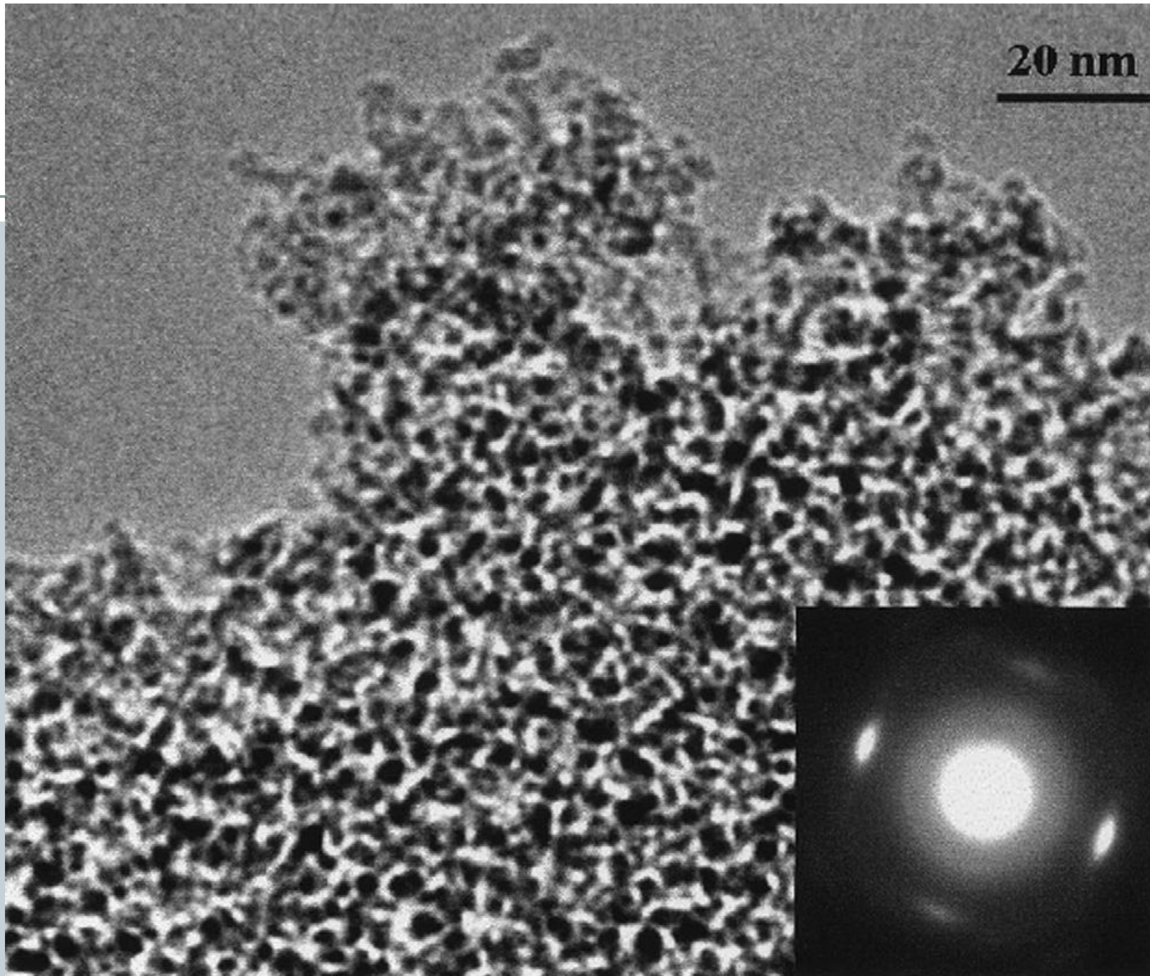
[2]*ST Microelectronics, 10 rue Thalès de Milet, 37071 Tours cedex 2, France*

The increasing expansion of telecommunication applications leads to the integration of complete system-on-chip associating analog and digital processing units. Besides, the passive elements occupy an increasing silicon footprint, compromising circuit scalability and cost. Moreover, passive components' performances are limited by the proximity of lossy Si substrate and surrounding metallization. Then, obviously, the characteristics of the substrate become crucial for monolithic radio frequency (RF) systems to reach high performances. So, looking for integrated circuit compatible processes, porous silicon (PS) seems to be a promising candidate as it can provide localized isolating regions from various silicon substrates. In this review, we first present all the possible porous silicon substrates, which can be used for RF devices. In particular, we put the emphasis on the etching conditions, leading to high thickness localized PS layers. The intrinsic electrical properties of porous silicon such as AC electrical conductivity or dielectric constant are also detailed, and the results extracted from the literature are commented. Then, we describe the performances of widespread RF devices, that is, inductors or coplanar waveguides. Finally, we describe methodologies used for predicting RF electrical responses of PS isolated devices, based on electromagnetic simulations. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4833575]



- Out-of-focus phase contrast micrographs of freshly cleaved fragments of microporous silicon layers, obtained from (100) p-type substrates.

JOURNAL OF APPLIED PHYSICS **121**, 104904 (2017)

Flexible hybrid circuit fully inkjet-printed: Surface mount devices assembled by silver nanoparticles-based inkjet ink

J. Arrese,[a] G. Vescio, E. Xuriguera, B. Medina-Rodriguez, A. Cornet, and A. Cirera
MIND–IN2UB, Department of Engineering: Electronics, Universitat de Barcelona, Martí i Franquès 1,

Nowadays, inkjet-printed devices such as transistors are still unstable in air and have poor performances. Moreover, the present electronics applications require a high degree of reliability and quality of their properties. In order to accomplish these application requirements, hybrid electronics is fulfilled by combining the advantages of the printing technologies with the surface-mount technology. In this work, silver nanoparticle-based inkjet ink (AgNP ink) is used as a novel approach to connect surface-mount devices (SMDs) onto inkjet-printed pads, conducted by inkjet printing technology. Excellent quality AgNP ink-junctions are ensured with high resolution picoliter drop jetting at low temperature (~150 °C). Electrical, mechanical, and morphological characterizations are carried out to assess the performance of the AgNP ink junction. Moreover, AgNP ink is compared with common benchmark materials (i.e., silver epoxy and solder). Electrical contact resistance characterization shows a similar performance between the AgNP ink and the usual ones. Mechanical characterization shows comparable shear strength for AgNP ink and silver epoxy, and both present higher adhesion than solder. Morphological inspections by field-emission scanning electron microscopy confirm a high quality interface of the silver nanoparticle interconnection. Finally, a flexible hybrid circuit on paper controlled by an Arduino board is manufactured, demonstrating the viability and scalability of the AgNP ink assembling technique. *Published by AIP Publishing*.

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Effectiveness of Stressors in Aggressively Scaled FinFETs

Nuo Xu, *Student Member, IEEE*, Byron Ho, *Student Member, IEEE*, Munkang Choi, Victor Moroz, and Tsu-Jae King Liu, *Fellow, IEEE*

***Abstract*—The stress transfer efficiency (STE) and impact of process-induced stress on carrier mobility enhancement in aggressively scaled FinFETs are studied for different stressor technologies, substrate types, and gate-stack formation processes. TCAD simulations show that strained-source/drain STE is 1.5× larger for bulk FinFETs than for SOI FinFETs. Although a gate-last process substantially enhances longitudinal stress within the channel region, it provides very little improvement in electron mobility over that achieved with a gate-first process. Guidelines for FinFET stressor technology optimization are provided, and performance enhancement trends for future technology nodes are projected.**

***Index Terms*—Carrier mobility, contact etch-stop layer (CESL), FinFET, gate first, gate last, Si:C, SiGe, source/drain (S/D) stressors, strain, stress transfer efficiency (STE).**

I. Introduction

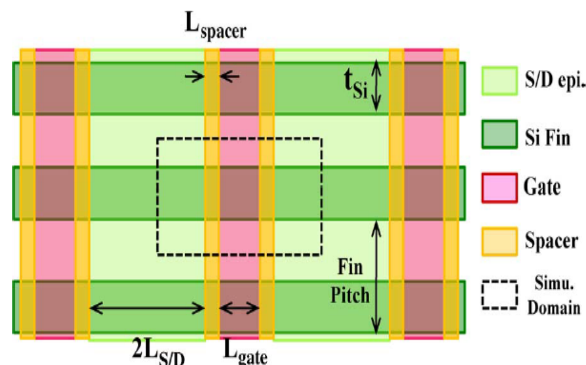
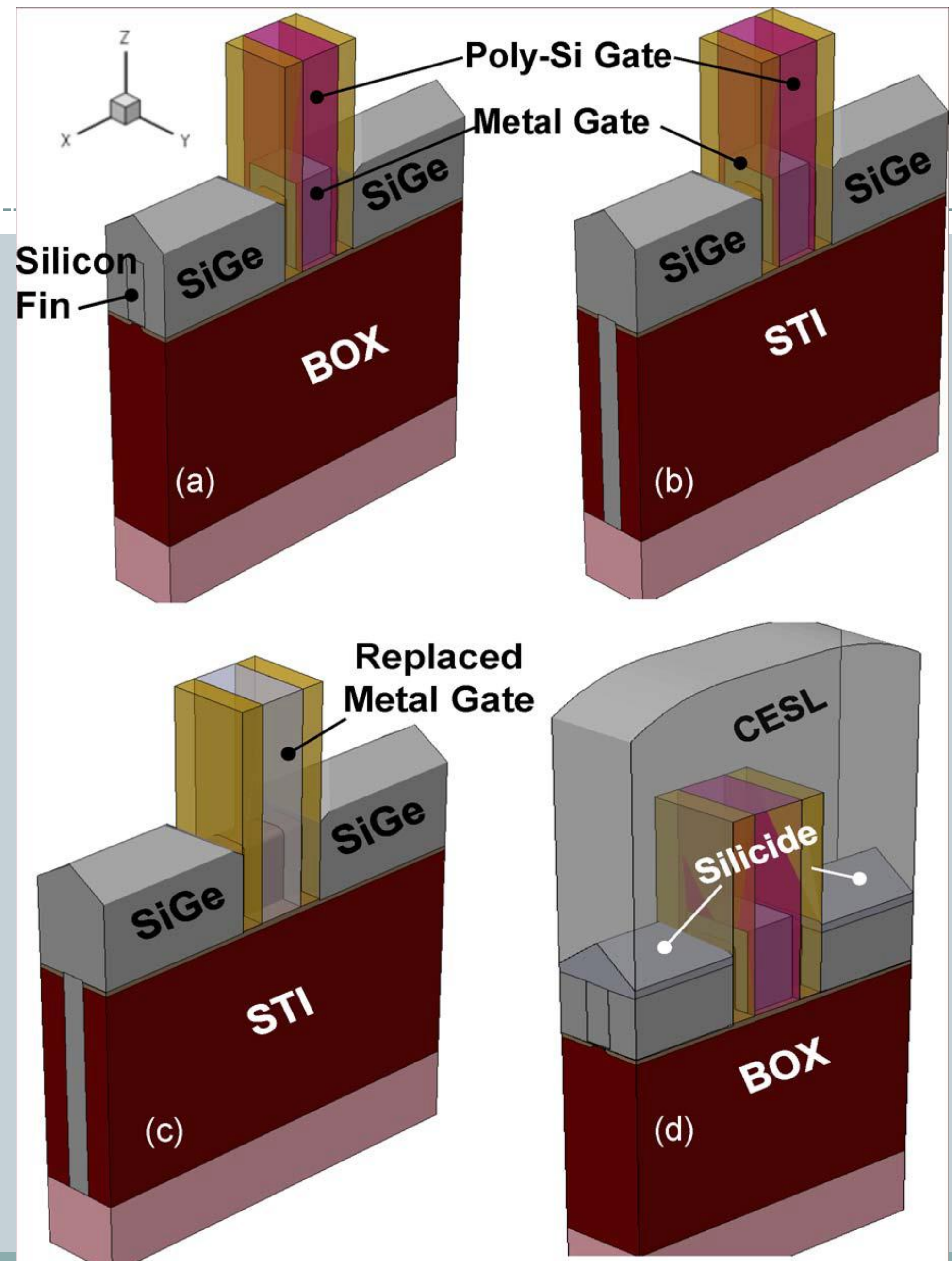


Fig. 1. Schematic plan view of FinFETs and region simulated in this work.

substrates and gate-first versus gate-last process integration schemes. The impact of the stressors on the effective carrier mobility is presented to evaluate their efficacy for boosting

CNT image - Google... Art_NANO_Eln Microsoft PowerPoin... Untitled - Paint Art_IEEE_2012_FinFET... EN 9:29 PM

- FinFET device structures studied in this work. (a) SOI FinFET with partially strained S/D.



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JOURNAL OF THE
ELECTRON DEVICES SOCIETY

Digital Object Identifier 10.1109/JEDS.2014.2328032

Graphene for Electron Devices: The Panorama of a Decade

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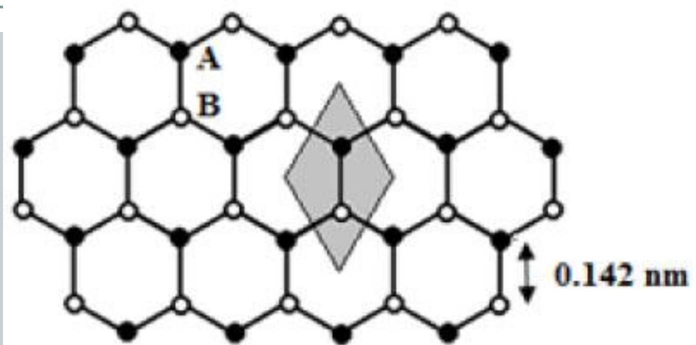
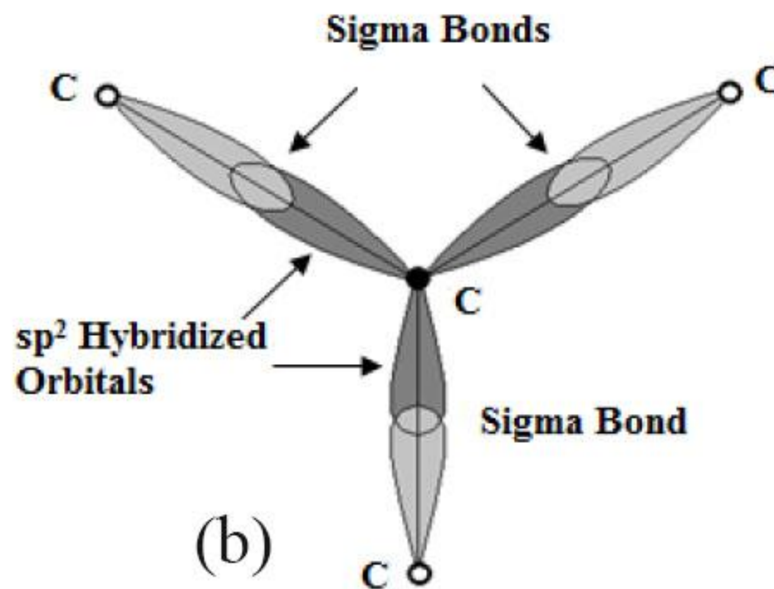
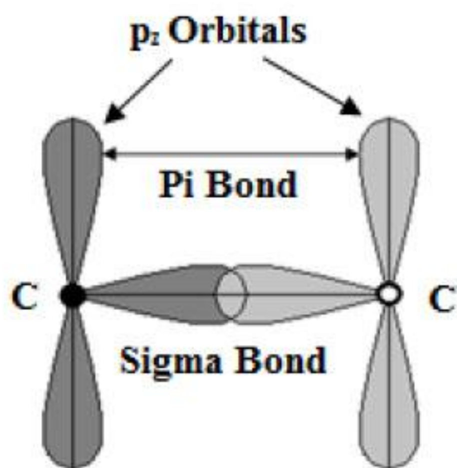
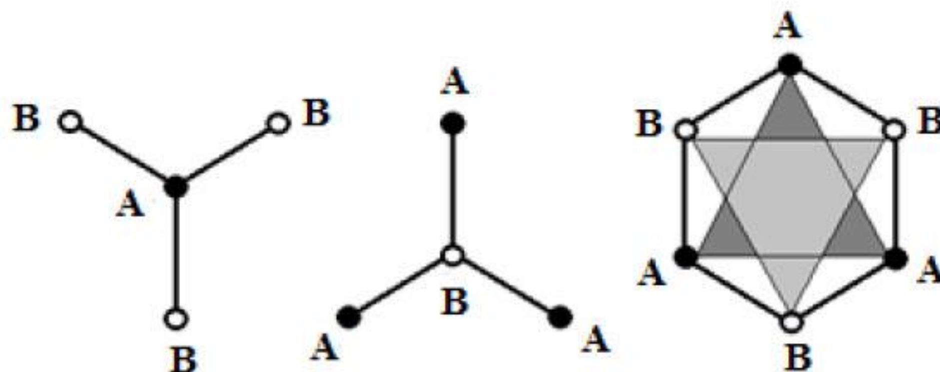
ABSTRACT Graphene emerged in 2004 as the first 2-D material with exotic properties. Since then the literature has been flooded with reports, with physicists, material scientists, and engineers grabbing their respective shares. Numerous reviews have also been published. While these reviews have done excellent works in their own ways, new reports are coming up faster than they could draw the attentions of researchers. The authors, therefore, feel that there is a demanding scope for a fresh review. Further, many aspects of graphene are not covered in the reviews so far. New concept devices are also entering into the arena of graphene day by day. The purpose of this paper is therefore to present a comprehensive review on the conventional as well as novel device applications of graphene. While we believe that graphene is the material which will transform the electron devices from the classical regime to the quantum world, it is difficult to believe that it will be a complete substitute to silicon in the near future.

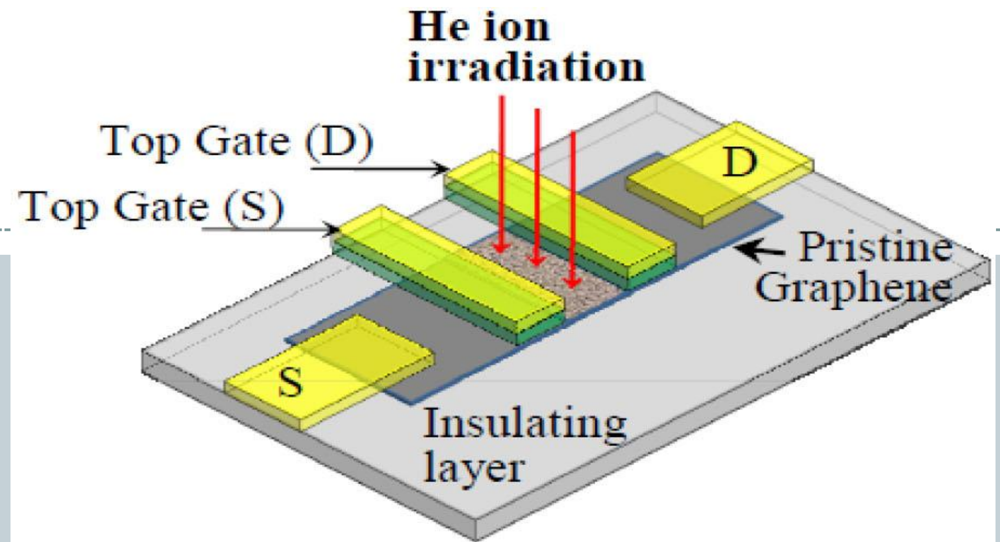

A
B
0.142 nm
(a)


Sigma Bonds
C
C
C
sp² Hybridized
Orbitals
Sigma Bond
(b)
C

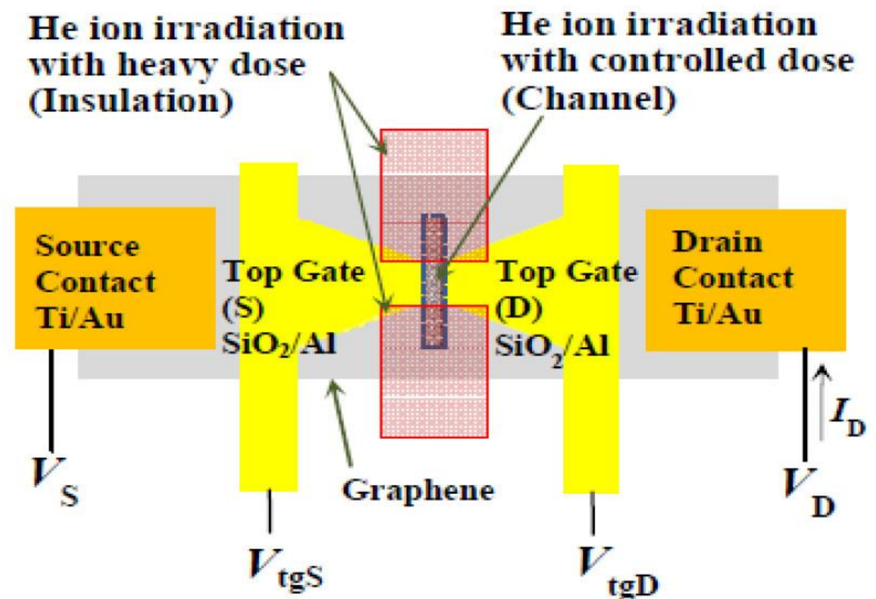

pz Orbitals
Pi Bond
C
C
Sigma Bond
(c)


B
B
A
B
A
A
B
A
A
B
B
A
A
B
(d)

- Double top-gated He ion irradiated graphene FET. (a) Schematic representation of the FET structure. (b) More detailed layout of the gates and graphene with heavy dose and controlled dose irradiation.



(a)



(b)

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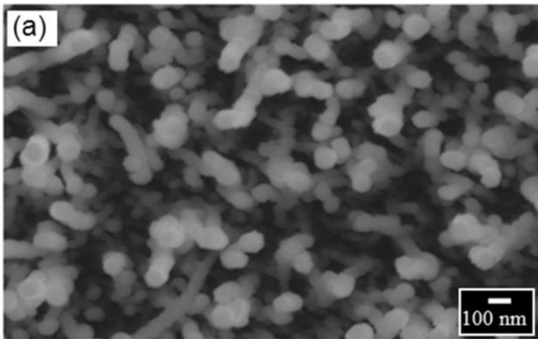
journal homepage: www.elsevier.com/locate/tsf

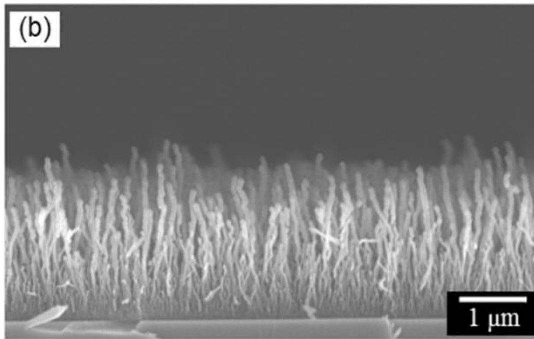
AlN film thickness effect on photoluminescence properties of AlN/carbon nanotubes shell/core nanostructures for deep ultra-violet optoelectronic devices

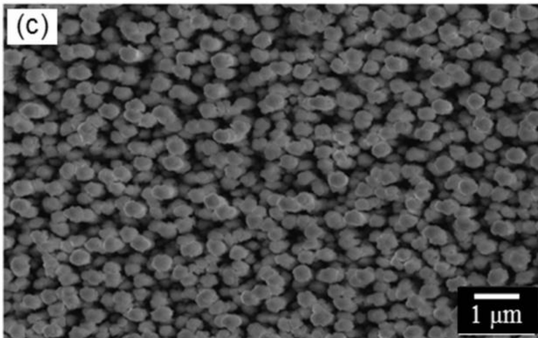
N. Ouldhamadouche [a,1], A. Achour [b,*,1], K. Ait. Aissa [c], M. Islam [d], A. Ahmadpourian [e], A. Arman [f], M.A. Soussou [g], M. Chaker [b], L. Le Brizoual [h], M.A. Djouadi [c]

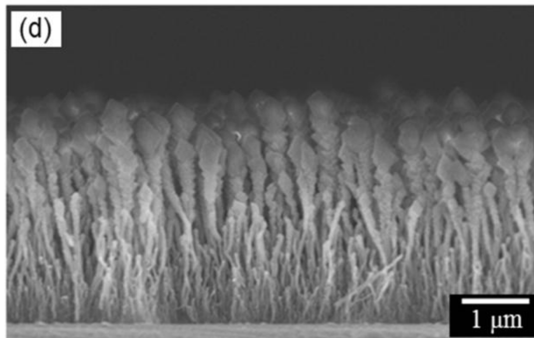
A B S T R A C T

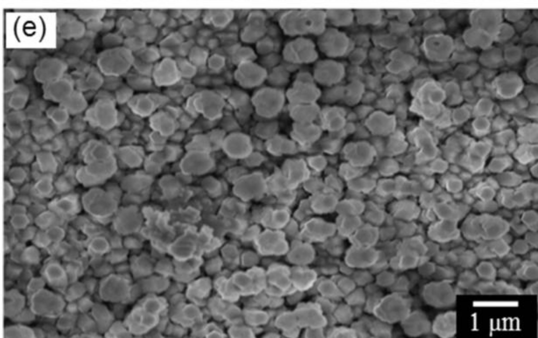
Aluminum nitride (AlN) nanostructures are very attractive in various optoelectronic applications such as deep ultraviolet light emitting devices. The fabrication of these AlN nanostructures with good crystalline quality and compatibility in line with other micro-fabrication processes has significant importance for practical applications. AlN films of different thickness values were deposited via DC reactive magnetron sputtering over vertically aligned multiwalled carbon nanotube (CNTs) arrays to obtain AlN/CNTs vertically-aligned shell/core nanostructure assembly. Such hybrid nanostructures were characterized using scanning electron microscope, transmission electron microscope, X-ray diffraction, Raman spectroscopy and time-resolved photoluminescence spectroscope (TR-PL) techniques. The results indicated that AlN/CNTs have a nanorods structure morphology with good AlN crystalline quality. The PL measurements revealed a maximum increase in the luminescent intensity of the exciton band in case of AlN/CNTs with 600 nm thick AlN layer, which is many orders of magnitude higher than that of AlN film produced over silicon substrate. It is anticipated that synergistic effects of CNTs and AlN through an increase in the specific surface area and oxygen-induced defects cause enhancement in the photoluminescence properties, making these hybrid nanostructures a promising candidate for optoelectronic applications.

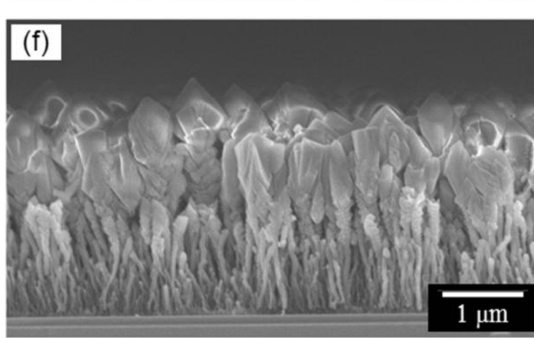


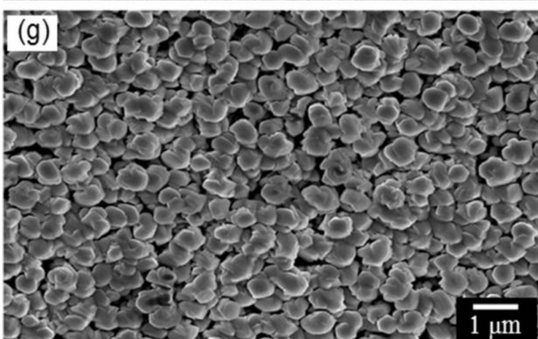


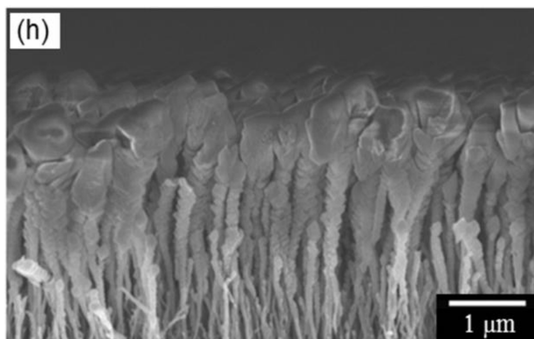












SEM images of the surface microstructure and cross-section of the AlN/CNT vertically aligned shell/core arrays with AlN film thickness of (a, b) 50 nm, (c, d) 400 nm, (e, f) 600 nm and (g, h) 1500 nm.

Realization and Scaling of Ge–$Si_{1-x}Ge_x$ Core-Shell Nanowire *n*-FETs

En-Shao Liu, David C. Dillen, Junghyo Nah, *Member, IEEE*, Babak Fallahazad, *Student Member, IEEE*, Kyounghwan Kim, and Emanuel Tutuc, *Senior Member, IEEE*

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 12, DECEMBER 2013

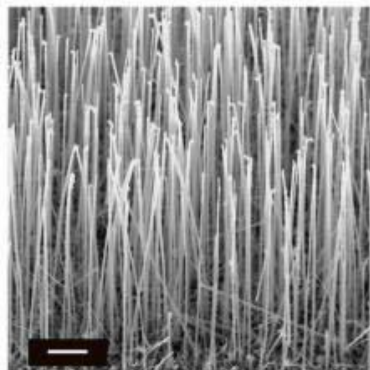
***Abstract*—We present the realization and scaling properties of germanium–silicon–germanium (Ge–$Si_{1-x}Ge_x$) core-shell nanowire (NW) *n*-type, Ω-gate field-effect transistors (FETs). The devices show superior performance to the counterparts without the $Si_{1-x}Ge_x$ shell. With a channel length (L_{ch}) of 380 nm and a diameter of 40 nm, we demonstrate a subthreshold swing of 180 mV/dec, and an ON-current (I_{ON}) of 60 μA/μm, comparable with recent results in Ge *n*-type FinFETs fabricated by top–down techniques. By systematically studying the scaling properties, we identify the contribution of the channel and contact resistances to device characteristics. We conclude that I_{ON} is not limited by the contact resistance but rather by a relatively large channel resistance, presumably associated with a high-interface trap density (D_{it}).**

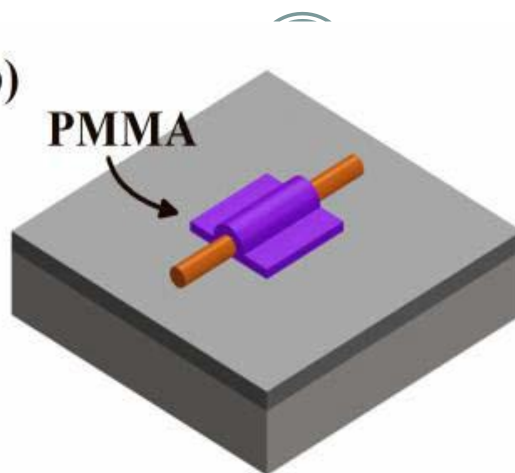
***Index Terms*—FinFETs, germanium, heterostructures, nanowires, silicon–germanium.**

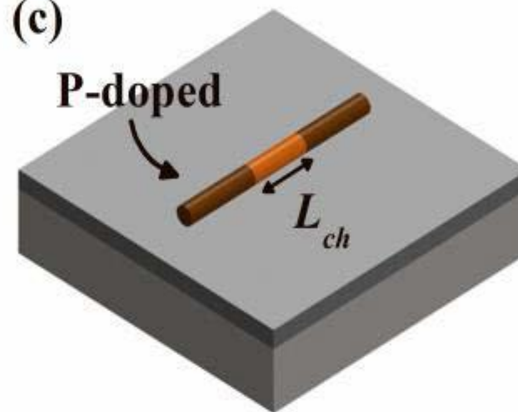
structure, in which the electrostatic control of gate over the channel potential is enhanced [15]. High-performance *p*-FETs on Ge–$Si_{1-x}Ge_x$ core-shell NWs have been demonstrated, showing high hole mobility thanks to the confinement provided by the valence band offset [16], [17]. In this paper, we investigate the potential of this material system for complimentary MOS technology by demonstrating the *n*-channel operation in Ge–$Si_{1-x}Ge_x$ NW FETs.

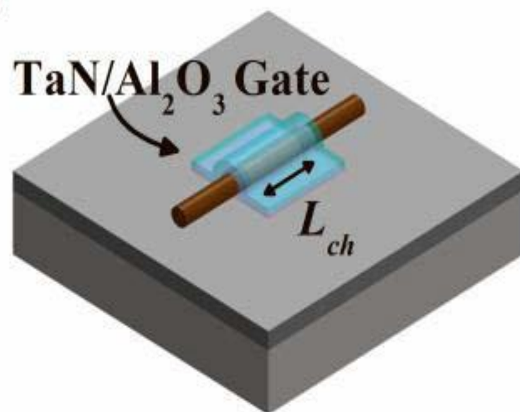
One typical problem of Ge *n*-FETs is the low drive current, which has been attributed partially to the large contact resistance (R_c) at the metal/Ge interface [18], [19]. Indeed, due to the lower *n*-type dopant activation levels in Ge [20] and Fermi level pinning [21], [22], the specific contact resistance (ρ_c) can be as large as 10^{-4} $\Omega\cdot cm^{-2}$ [18].

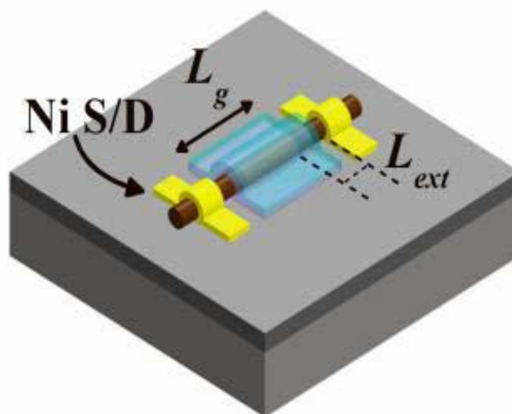
- Process flow for NW *n-FETs. (a) SEM of the core-shell NWs epitaxially grown on a Si (111) substrate.*
- *(b) PMMA is used* as the mask for P-implantation; the exposed NW sections represent the S/D regions.
- (c) PMMA removal and dopant activation anneal define the S/D. The channel (*Lch) is defined by the previously masked region.*
- *(d) Al_2O_3 and TaN are then deposited to form the gate-stack.*
- *(e) S/D contacts are formed by EBL,* Ni deposition and lift-off. Each fabricated device has the same *Lext and contact width.*
- *(f) SEM of a completed device. The yellow (blue) areas represent the* contact (gate) metal. The NW sections that receive P-implantation are highlighted in red.
- The scale bar is 500 nm.

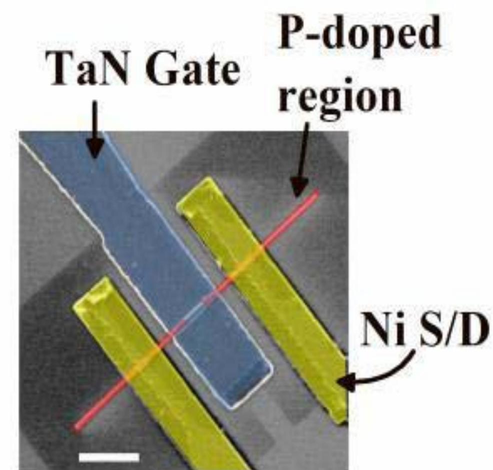

(a)


(b)
PMMA


(c)
P-doped
L_{ch}


(d)
TaN/Al_2O_3 Gate
L_{ch}


(e)
L_g
Ni S/D
L_{ext}


(f)
TaN Gate
P-doped
region
Ni S/D

Top-Down Fabrication of Epitaxial SiGe/Si Multi-(Core/Shell) p-FET Nanowire Transistors

Sylvain Barraud, Jean-Michel Hartmann, Virginie Maffini-Alvaro, Lucie Tosti,
Vincent Delaye, and Dominique Lafond

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 61, NO. 4, APRIL 2014

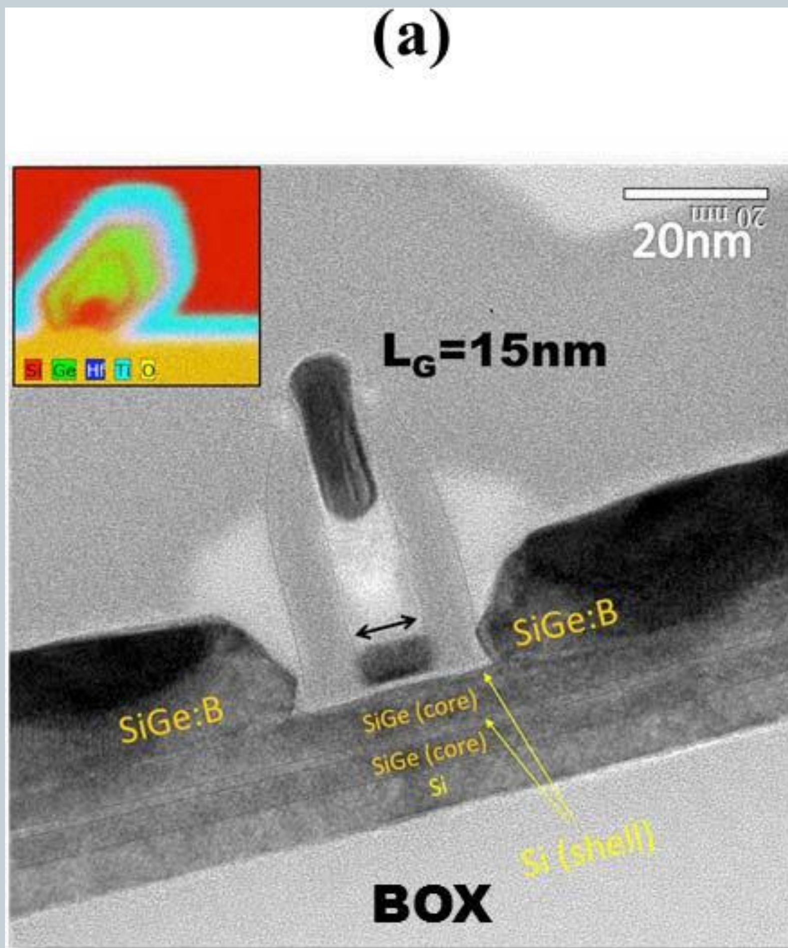
Abstract—**Short-gate length epitaxial $Si_{1-x}Ge_x$/Si multi-(core/shell) p-type nanowire (NW) transistors with high-permittivity dielectric and metal gate were fabricated and their electrical properties examined. Silicon NWs were first of all patterned in ultrathin silicon-on-insulator wafers by lithography and etching. Selective epitaxial growth of $Si_{0.7}Ge_{0.3}$/Si or $Si_{0.7}Ge_{0.3}$/Si/$Si_{0.7}Ge_{0.3}$/Si shells was then performed around the Si NW core. Electrical transport measurements showed a hole mobility improvement up to 100% in $Si_{0.7}Ge_{0.3}$/Si/$Si_{0.7}Ge_{0.3}$/Si core/shell NWs (70% in wide planar devices) compared with p-type Si reference field effect transistors (FETs). Finally, a drive current enhancement of 60% compared with reference Si-channel devices was evidenced in multi-(core/shell) p-FET NWs scaled down to 15-nm gate length.**

Index Terms—Compressive strain, core/shell, MOSFET, nanowire (NW), SiGe, silicon-on-insulator (SoI).

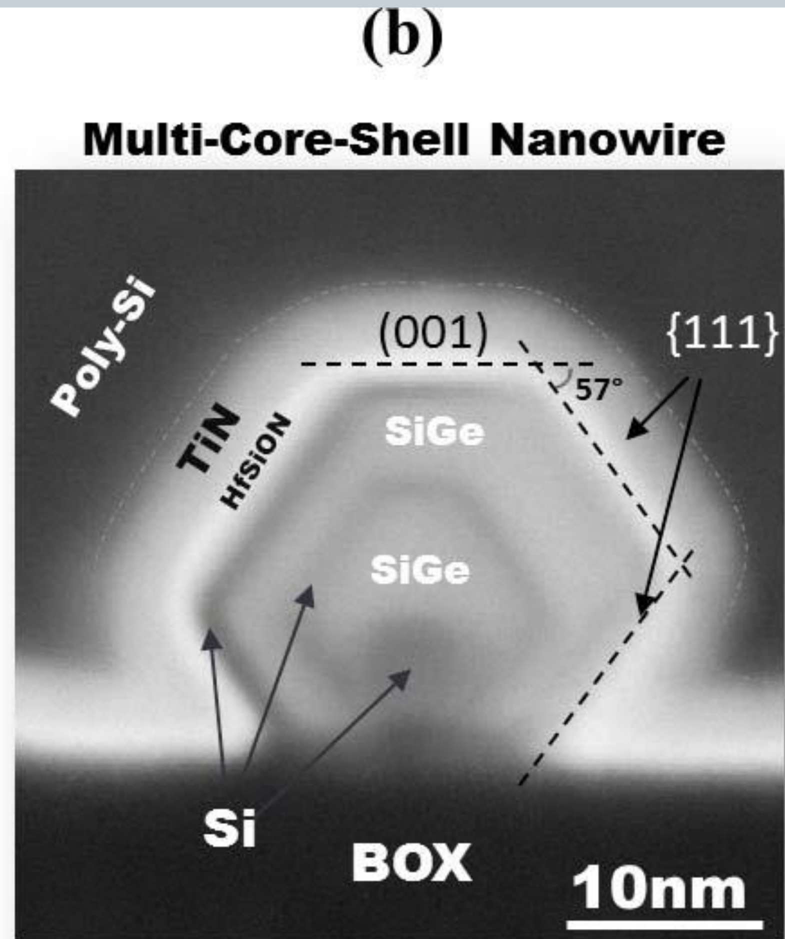
are plagued by low I_{ON}/I_{OFF} ratios due to a number of still standing issues associated with the integration of bottom-up semiconductor NWs [13]. Other integration schemes compatible with the standard CMOS technology (top-down approach) have been used for the fabrication of p-type SiGe/Si core/shell NW transistors [6], [7]. In this paper, radial heteroepitaxial growth of strained-SiGe multilayers on Si NW is demonstrated for the fabrication of p-type NW MOSFETs with high mobility channel. The $Si_{1-x}Ge_x$/Si strained heterostructure is used to create one or multiquantum wells in the NW cross section to improve the drain current level of transistors while keeping a good electrostatic control. For the first time, epitaxial growth of Si-cap/$Si_{0.7}Ge_{0.3}$/Si/$Si_{0.7}Ge_{0.3}$/Si multilayers is demonstrated for the fabrication of multi-(core/shell) NW transistors

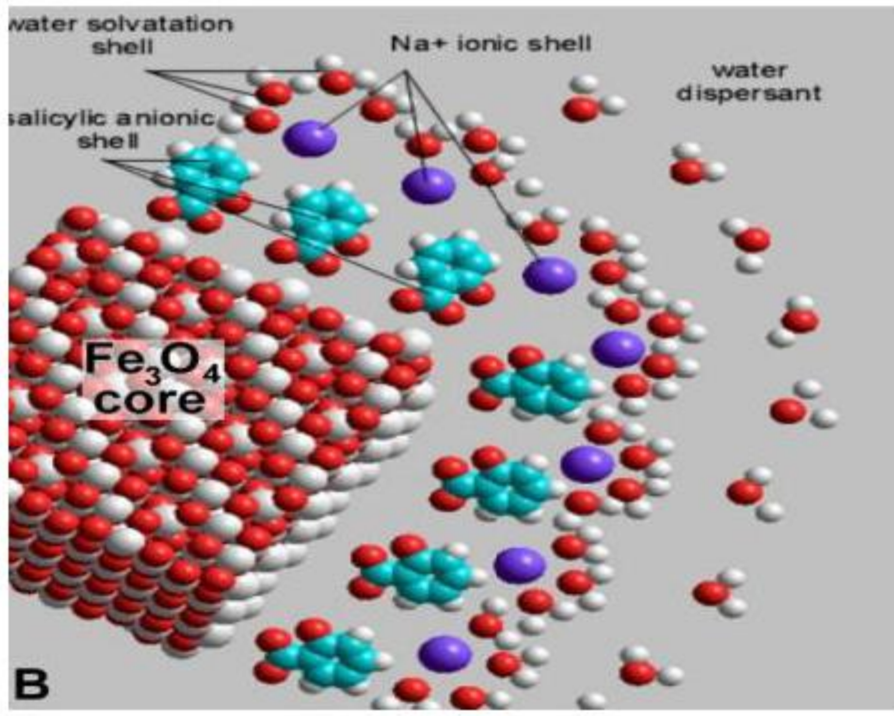
Cross-sectional TEM image of a SiGe/Si multi-(core/shell) p-FET NW transistor with a 15-nm gate length (inset: energy dispersive X-ray analysis of SiGe/Si multilayers with a HfSiON/TiN metal gate).
(b) Cross section of a hexagonal multi-(core-shell) NW

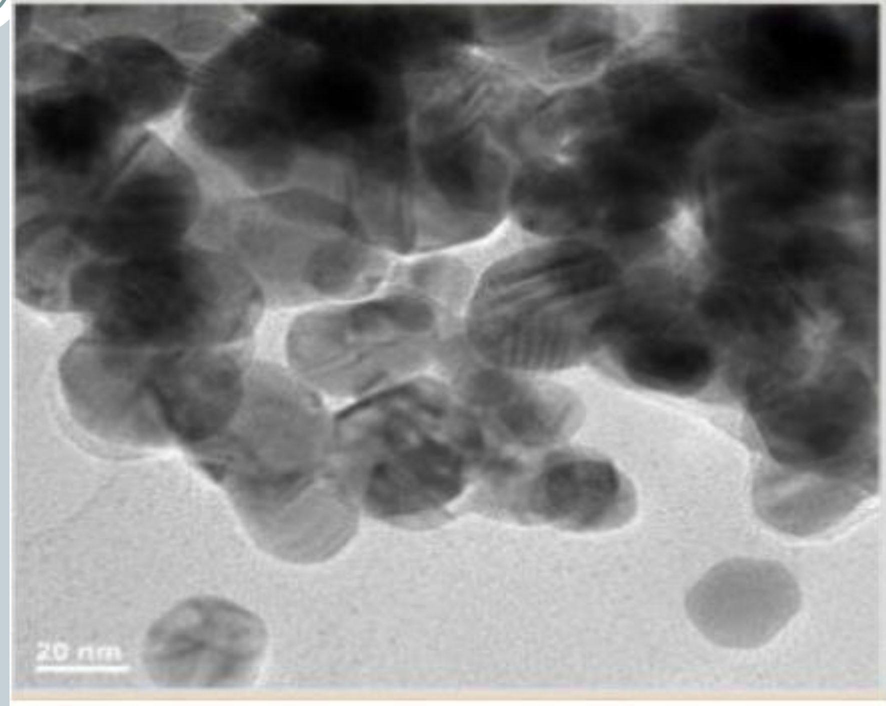
(a)



(b)





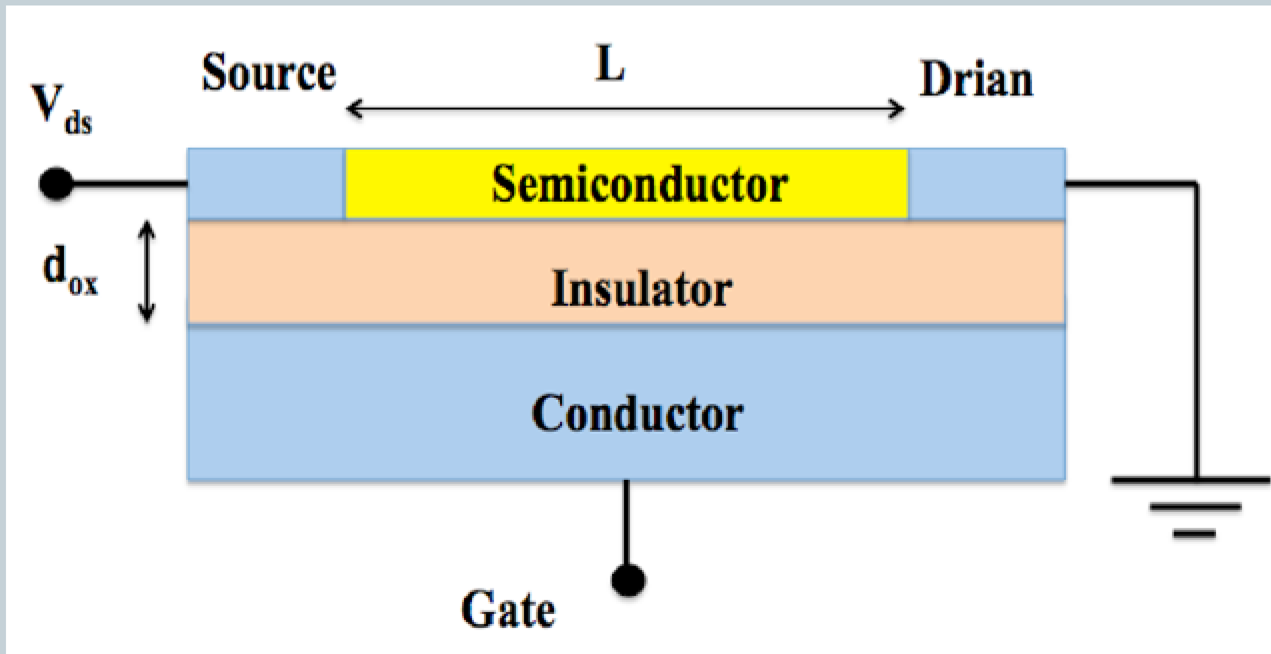


(a) The hydration shell; (b) Fe2O3 coated by p-aminobenzoic acid

1.3. Incadrarea tranzistoarelor cu filme subtiri TFT

- A thin-film-transistor (TFT) consists of a conductor called the gate (made of metal or a highly doped semiconductor) an insulating layer (which we will call the oxide layer, as an inheritance from silicon technology) of thickness *dox (resulting in capacitance density* $C_{ox} = \varepsilon_{ox}/d_{ox}$*, with* ε_{ox} *the permittivity of the insulator material) and a* semiconducting layer that accommodates the channel of charged carriers and is called the active layer.

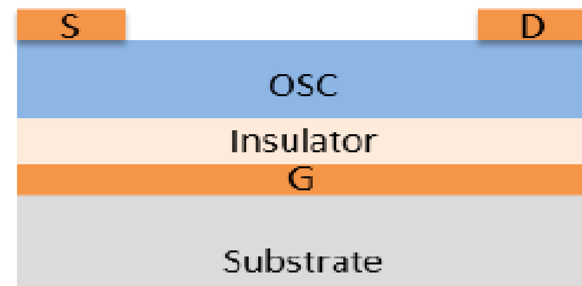
1.3. Incadrarea tranzistoarelor cu filme subtiri TFT



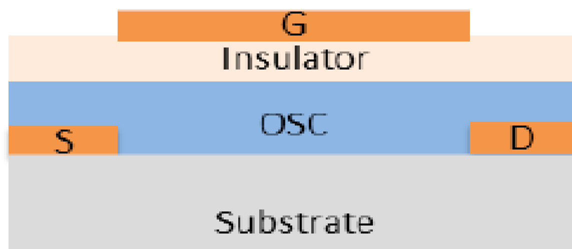
1.3. Incadrarea tranzistoarelor cu filme subtiri TFT

Schematic cross-section of common TFT structures: a) bottom-gate and bottom-contact; b) bottom-gate and top contact; c) top-gate and bottom contact, and d) top-gate and top contact.

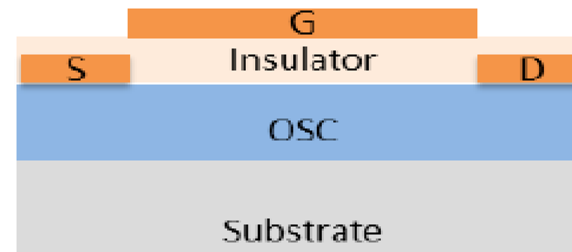
(a)



(b)



(c)



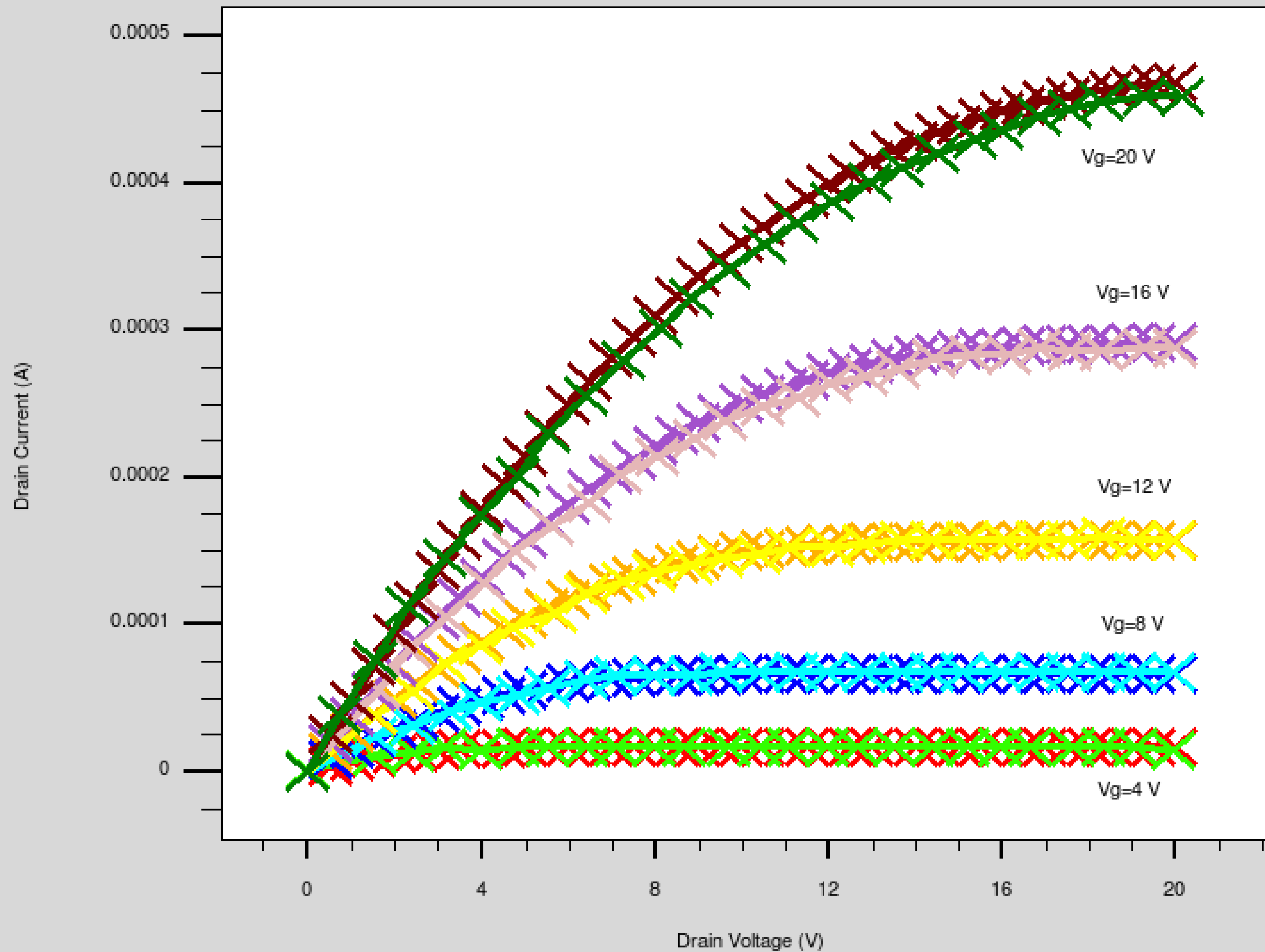
(d)

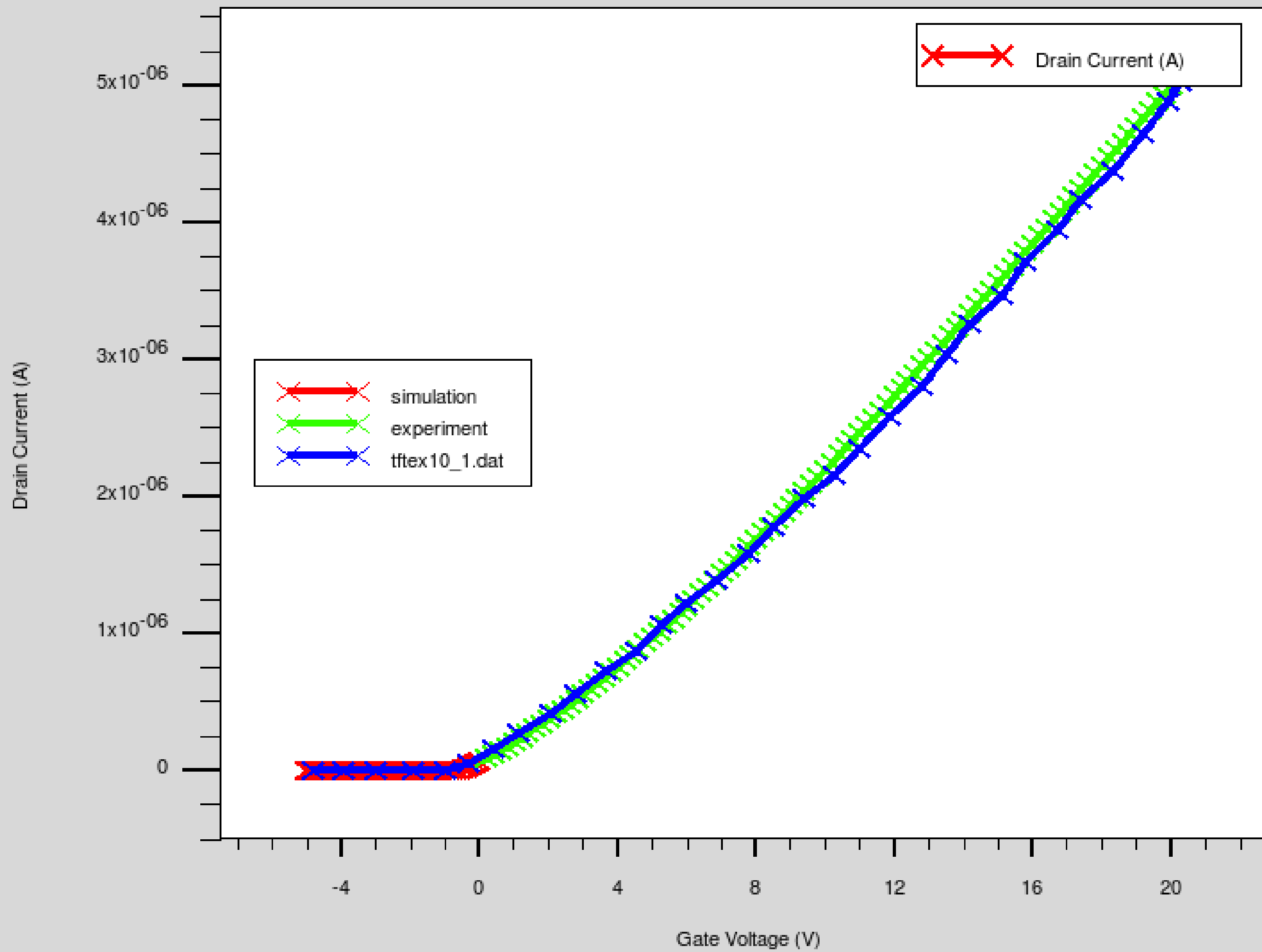
1.3. Incadrarea tranzistoarelor cu filme subtiri TFT

- TFT device with material properties corresponding to passivated alpha-Si:H material.

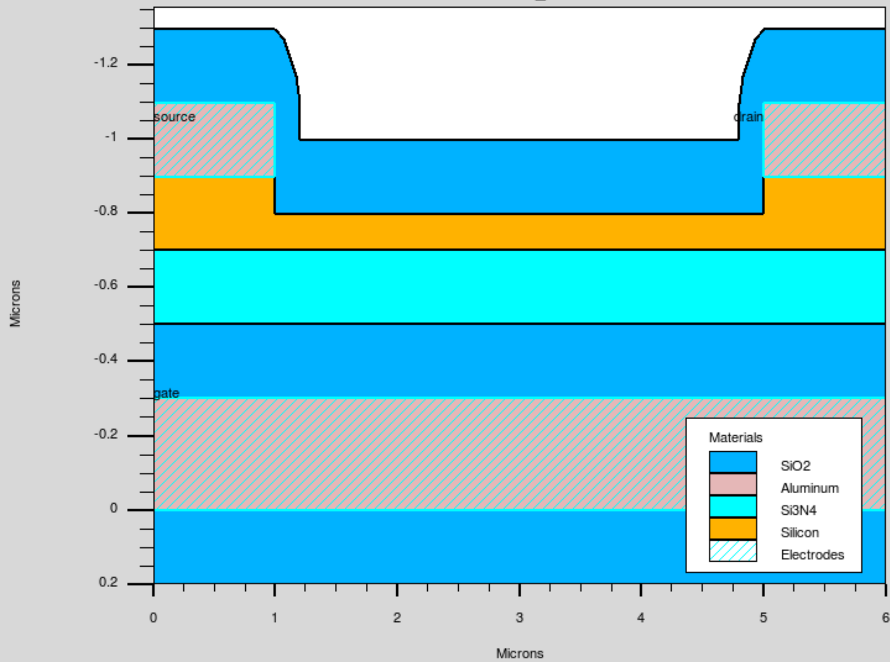
- TFT device with material properties corresponding to amorphous IGZO (indium galium zinc oxide) material.

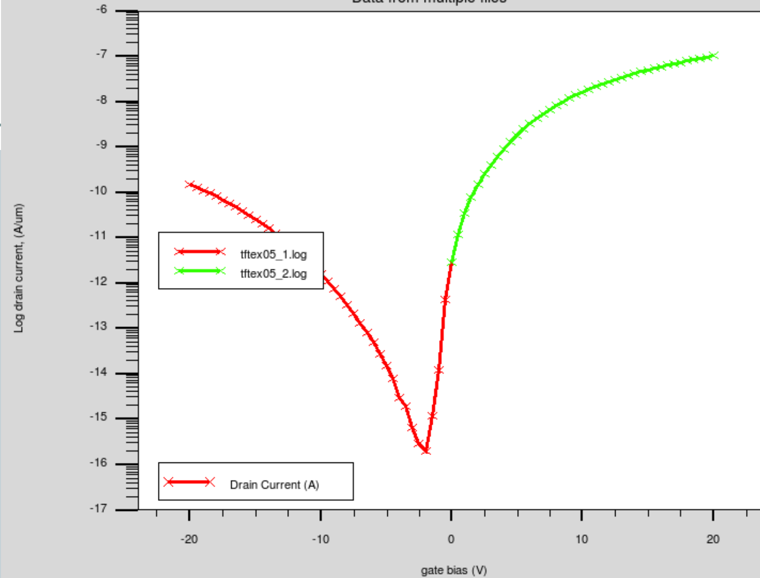
- The key command in TFT simulation is the **defect** statement. It is used to define a continuous density of trap states in the silicon and the relevant trapping cross-sections.


ATLAS simulation of amorphous IGZO TFT
Comparison of experiment and simulation
Drain Current (A)
0.0005
0.0004
0.0003
0.0002
0.0001
0
Vg=20 V
Vg=16 V
Vg=12 V
Vg=8 V
Vg=4 V
0
4
8
12
16
20
Drain Voltage (V)



ATLAS simulation of amorphous IGZO TFT
Comparison between simulation and experiment
Drain Current (A)
simulation
experiment
tftex10_1.dat
Drain Current (A)
5x10-06
4x10-06
3x10-06
2x10-06
1x10-06
0
-4
0
4
8
12
16
20
Gate Voltage (V)


ATHENA
Data from tftex05_0.str
source
drain
gate
Materials
SiO2
Aluminum
Si3N4
Silicon
Electrodes
Microns
Microns


ATLAS OVERLAY
Data from multiple files
tftex05_1.log
tftex05_2.log
Drain Current (A)
Log drain current, (A/um)
gate bias (V)